Optical Lithography Cost of Ownership (COO) – Final Report for LITG501

International SEMATECH

Technology Transfer # 00104014A-TR

Optical Lithography Cost of Ownership (COO) – Final Report for LITG501

Technology Transfer # **00104014A-TR**
International SEMATECH
October 31, 2000

Abstract: This final report from the LITG501 project presents an overview of the results of the latest formal revision of the lithography cost of ownership (COO) model, which compares costs of competing technologies without bias. This report focuses on the four principal drivers of the final COO results: mask usage, mask cost, tool throughput, and tool cost. For manufacturers with low mask usage, the mask write step is the biggest driver of wafer-level COO. Manufacturers with high mask usage should concentrate improvement efforts on tool throughput and tool cost. Costs will continue to be driven upwards when changing to 300 mm wafers.

Keywords: Cost Modeling, Cost of Ownership, Lithography, Masks, Throughput

Authors: Ed Muzio

Approvals: Ed Muzio, Project Manager
Gerhard Gross, Director
Laurie Modrey, Technical Information Transfer Team Leader

Table of Contents

List of Figures

List of Tables

1 OVERVIEW

International SEMATECH uses a detailed lithography cost of ownership (COO) modeling technique to compare the cost ramifications of competing future technologies in an equivalent, unbiased manner. Given a variety of input parameters and assumptions, the cost of one good wafer level exposure (GWLE) through exposure tool and track can be calculated. To make this possible, several simplifying assumptions must be made, along with a large number of controversial parameter estimates. To remain unbiased and abreast of the latest technical developments, International SEMATECH uses a periodic formal review process in which all of the COO assumptions are reviewed, documented, and published on a public website (http://www.sematech.org/public/resources/coo/index.htm). This makes it possible for individual users to review the analysis and understand what modifications are necessary to apply the International SEMATECH "generic" analysis to a specific case. Users are cautioned, however, that the point of the analysis is to compare alternatives and identify key cost contributors and that resulting cost estimates should never be directly used for business planning.

Although the wafer-level cost calculation requires many parameters, the four principal drivers of the final COO results are mask usage, mask cost, tool throughput, and tool cost. These parameters are the focus of this report. Those who are interested in any of the other myriad parameters can review them in detail on the COO website.

This final report documents at a high level the results of the latest formal revision, December 1999, at the time of the closing of project LITG501. This work continues within the International SEMATECH Advanced Lithography Thrust and is now managed by Walt Trybula, (512) 356-3306, walttrybula@sematech.org.

2 COST PARAMETERS

2.1 Mask Usage

Mask usage is defined as the number of wafers that are exposed by a single mask during its whole lifetime. Because the cost of the mask is spread over the number of wafers it exposes, the sensitivity to both mask usage and mask cost is significantly greater in low mask-usage regimes. Figure 1 shows this relationship. Generally speaking, DRAM and microprocessor manufacturers tend to have high mask usage values, while ASIC and logic manufacturers operate on the lower end of the spectrum. For this reason, International SEMATECH publishes all COO results at both low usage (500 wafers per mask [WPM]) and high usage (8000 WPM) levels. These levels are believed to be indicative of the bimodal industry "averages," as indicated by response levels to a recent industry survey (see Figure 2).

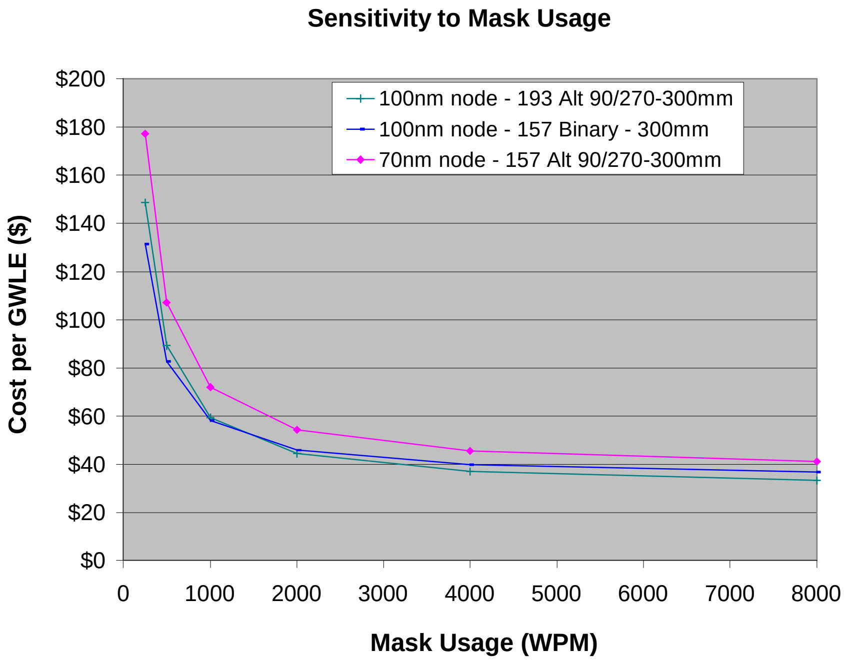

Figure 1 COO Sensitivity to Mask Usage

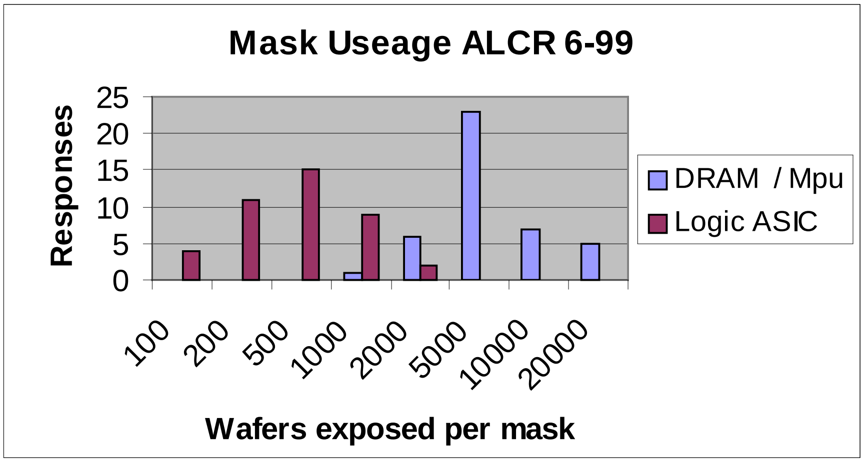

Figure 2 Industry Survey Results Regarding Mask Usage

2.2 Mask Cost

Mask cost, the cost to obtain the mask itself, also impacts final wafer-level cost. This impact is predictably reduced in high mask usage scenarios where the mask cost is spread over many wafers (see Figure 3).

Mask costs are estimated by modeling the mask-making process assuming a production volume of 100 masks per week of a single mask type. Such simplifying assumptions may not reflect reality, but are necessary to facilitate comparative modeling. They do not, however, compromise the model’s ability to identify mask cost drivers, which is one of the key purposes of the modeling. Figure 4 shows these key contributors to mask cost, all of which translate directly to higher wafer level costs, especially if mask usage levels are low. For each cost driver, the graph shows the overall cost savings if that particular issue were removed completely from the mask manufacture process.

Highest on this “Pareto” of mask cost effects is the mask write step. Even though the analysis makes aggressive assumptions on mask writer costs and throughput based upon historical learning, the resulting mask writer contribution is still extremely high. In fact, it accounts for upwards of 50% of the total cost contribution of every tool in the mask shop (see Figure 4). It is worth noting that these results remain even after significant decreases to the overall COO of the mask write step were implemented in the December 1999 COO revision. Before this revision, capital cost and write times were significantly longer, resulting in a total mask cost even more heavily impacted by the write step.

Figure 4 also identifies blank cost and process yield as two key cost contributors. In this arena as well, significant improvements were made in the December 1999 revision, with cumulative process yields going from the 50% range to the 70% range as specified by a panel of mask making experts. Even so, these yields create an obvious cost driver, compounded by the fact that the losses are taken on expensive mask blanks that, for the most part, cannot be recycled.

Mask yields themselves are a modeling challenge within the overall challenge of the COO modeling. The general strategy in modeling mask yield values is to assume that, in the absence of any significant technological changes, the mask industry will continue to “learn” at the same rate as it has in the past. Thus it is assumed that the third year production yields will tend toward today’s third year production values. The challenge, then, becomes how to consistently and qualitatively account for the inevitable technological changes that will impact this learning assumption. The COO website contains more detail on how this is accomplished, in a way that is as consistent as possible with today’s knowledge and the expected technological variations fin the future.

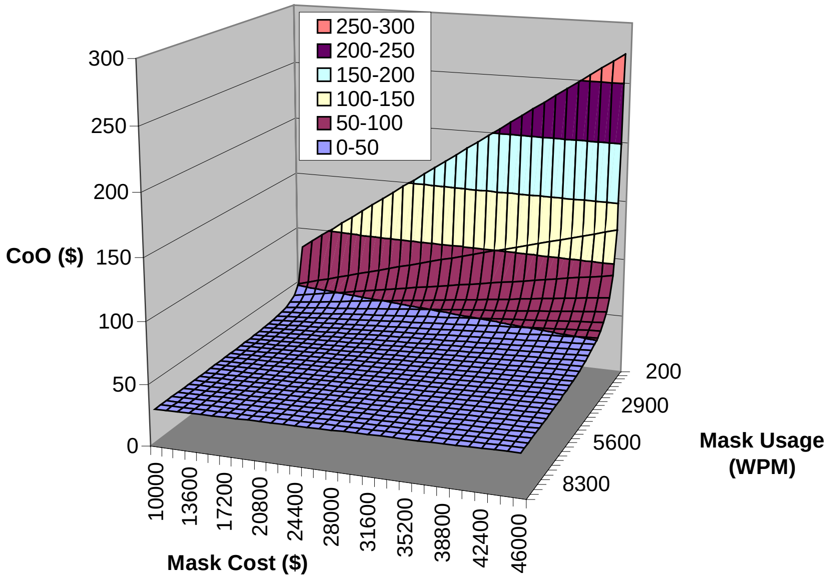

Figure 3 COO Sensitivity to Mask Cost and Mask Usage

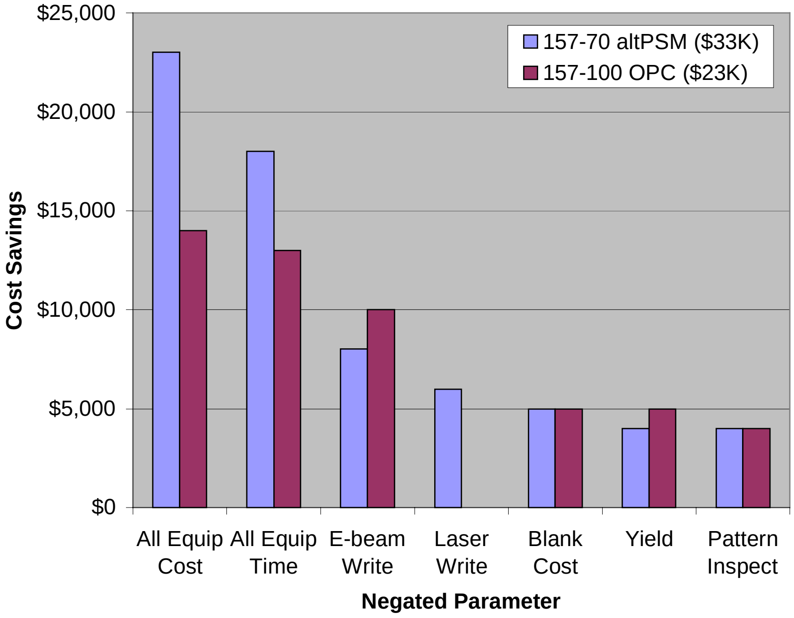

Figure 4 Key Drivers to Mask Cost

2.3 Tool Throughput

The throughput of the exposure system is the third key lever to wafer-level cost. SEMATECH assumes an exposure tool-limited throughput (as opposed to a track-limited throughput) and uses technology-specific modeling to predict the throughput in each case. The detailed inputs to that model are available on the web site, but the resulting sensitivity is worth noting and is included here.

Figure 5 shows the final cost sensitivity to wafer-level throughput. One key result of the throughput sensitivity is that there is no regime in the cost model in which a dual (trim) mask approach to a phase shift mask strategy is more advantageous than a single mask approach. As the dotted line in Figure 5 shows, any potential reticle savings will be offset at the wafer level by the increased COO due to the throughput reduction. Thus the conclusion from this work is that if there is justification for a two-mask approach, it will have to come from wafer yield or device performance, not from basic cost of ownership.

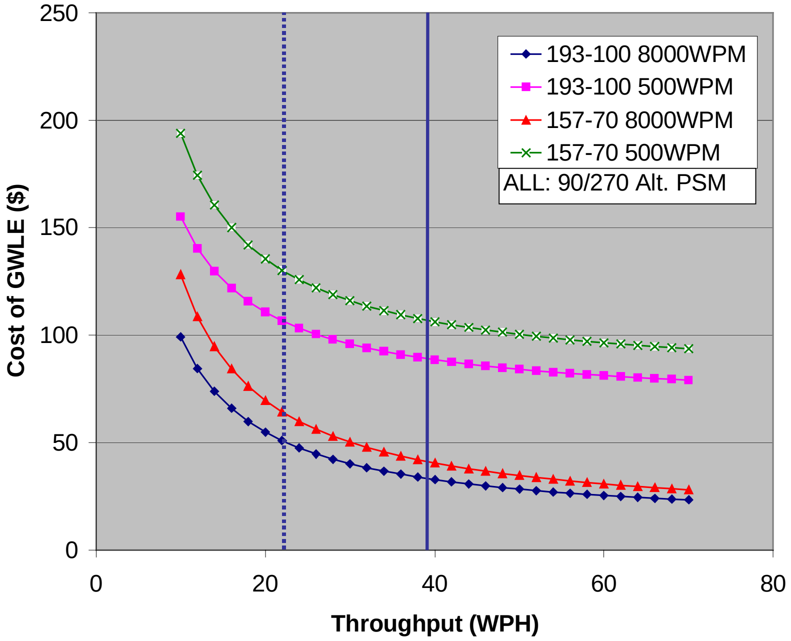

Figure 5 COO Sensitivity to Tool Throughput

In throughput, all technologies are faced with the tradeoff of resist sensitivity for available dose. For 157 nm and 193 nm optical lithography, for example, higher rep-rate lasers and pulse stretching may be required to meet throughput and resist requirements.

2.4 Tool Cost

The final key driver of wafer-level COO is the capital cost of the tool itself. The impact of tool cost is closely coupled to throughput. Higher throughput systems are less sensitive to overall tool cost since the cost of the system is spread over more wafers (see Figure 6). In tool cost, the largest single factor that needs to be attacked is the requirement for larger field sizes that are not actually used. This is a major issue with high numerical aperture (NA) optical systems where lens costs could be reduced if the field size requirements were specified accurately. Some estimates indicate that the reduction could be by as much as a factor of 2.6

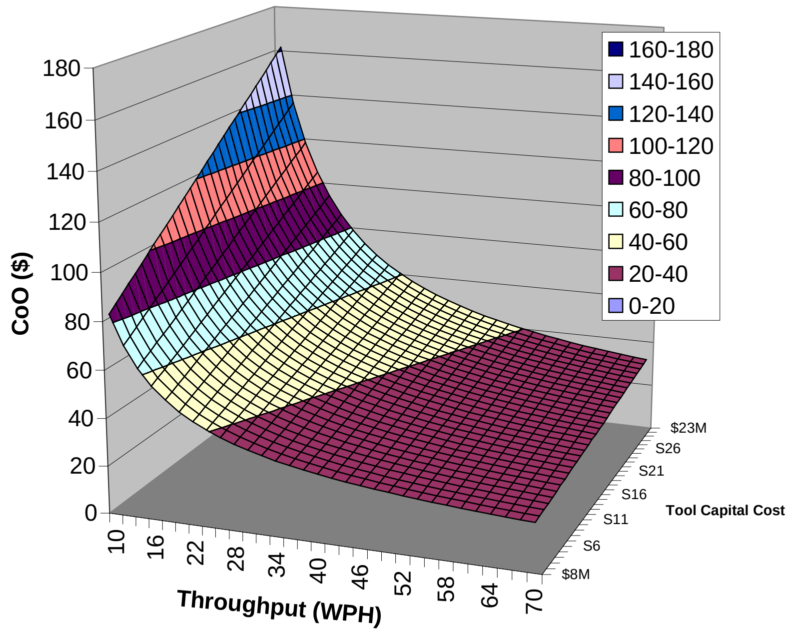

Figure 6 COO Sensitivity to Tool Throughput and Capital Cost

Tool costs for future optical systems are modeled using a combination of historical trend and technical and business information from the industry. Figure 7 shows the assumed future tool costs (for all nodes) from the December 1999 COO revision. It is worth noting that the forecasted tool costs are well within the historical trend, but on the low side due to the expectation that competitive pressure will ultimately end the exponential tool cost growth trend.

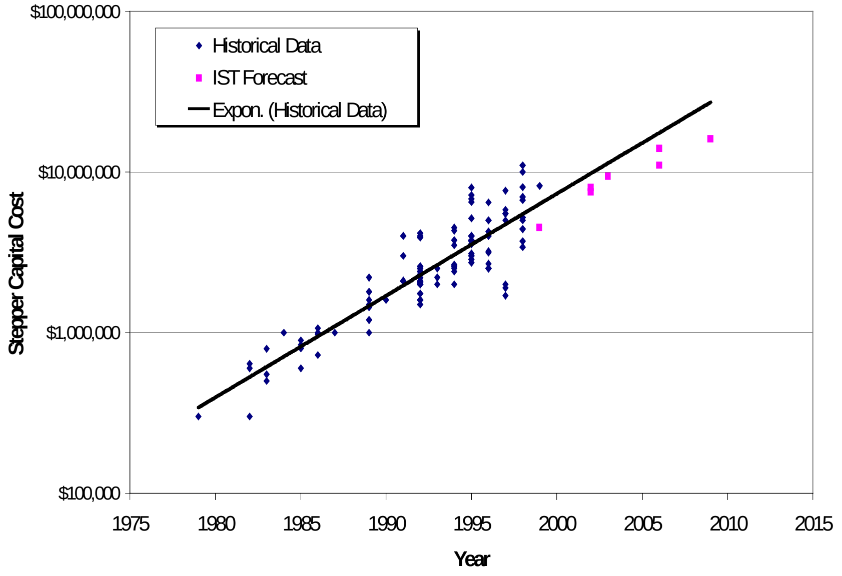

Figure 7 Projected Tool Costs (all nodes) and Historical Trend

3 RESULTS

The current analysis indicates that the cost of lithography will continue to increase in the future. Table 1, taken from Technology Transfer #00013884A-TR (LITG500), shows projected GWLE cost for optical lithography at the 100 nm and 70 nm nodes on 300 mm wafers. The trend from today's costs is clearly upwards. Part of this upward trend is driven by the change to 300 mm, which raises wafer processing costs but also increases amount of revenue per wafer (see the 130 nm node example, Table 2). The balance of the increase is due primarily to the four key drivers detailed in this report.

Table 1 Final COO Analysis Results (December 1999)

100 nm Node – 300 mm Wafers					
Technology	**Reticle**	**Tool**	**TPT (wph)**	**COO 500 WPM**	**COO 8000 WPM**
193 nm Alternating PSM	$28K	$11M	38.9	$89	$33
157 nm Binary w/OPC	$23K	$14M	38.9	$83	$37
70 nm Node – 300 mm Wafers					
Technology	**Reticle**	**Tool**	**TPT**	**COO**	**COO**
157 nm Alternating PSM	$33K	$16.1M	38.9	$107	$41

ESTIMATES ONLY, NOT FOR BUSINESS PLANNING PURPOSES

Table 2 Comparison of 200 mm and 300 mm COO at the 130 nm Node

	200 mm	300 mm	Change
Throughput (WPH)	62.7	38.9	-62%
COO @ 500 WPM	$58	$66	+114%
COO @ 8000 WPM	$22	$30	+136%
Fields Per Wafer	37	89	+241

ESTIMATES ONLY, NOT FOR BUSINESS PLANNING PURPOSES

4 CONCLUSION

COO analysis is a valuable way to identify cost reduction areas in every technology. Current estimates indicate that mask cost, tool cost, and tool throughput continue to be the areas of high concern across all optical technology options. For manufacturers with low mask usage, the single biggest driver to wafer-level COO continues to be the mask write step. Manufacturers with high mask usage, on the other hand, should concentrate improvement efforts on tool throughput and tool cost. In either case, the cost tradeoff indicates no support of a dual-mask approach to phase shift masks because of the associated throughput decrease. Going forward, the areas in which action should be focused are best selected using a COO analysis such as the one presented here. In this way, the industry can ensure that it will meet the business challenges as well as the technical challenges as requirements advance.

International SEMATECH Technology Transfer
2706 Montopolis Drive
Austin, TX 78741

http://www.sematech.org
e-mail: info@sematech.org