



**Understanding and Developing Knowledge-based Qualifications of
Silicon Devices**

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**Understanding and Developing Knowledge-based Qualifications of
Silicon Devices
Technology Transfer #04024492A-TR
International SEMATECH
March 30, 2004**

Abstract: Knowledge-based reliability qualification differs from standards-based methods in that it comprehends the end-user environment and failure mechanism based-methods. With this approach, the challenges and tradeoffs of qualification can be more flexibly addressed than with a standards-based approach. Understanding interrelationships of design, technology, manufacturing, and product attributes is essential. Risk management should be viewed as an integral element. Critical considerations for developing a knowledge-based qualification (KBQ) plan include selecting technology- and product-relevant structures for reliability evaluation and establishing assessment models and criteria for them. Further discussion and observations about using the KBQ approach include the extrapolation of results from test structures to products and the problem that accepted failure models may not be available. Some brief examples of KBQ are given.

Keywords: Reliability Testing, Test Methods, Qualification Plan, Risk Management

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Acknowledgments

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1 EXECUTIVE SUMMARY

The differences between stress-based and knowledge-based qualification (KBQ) methodologies are compared and discussed, highlighting the weaknesses of a stress-based approach and merits of knowledge-based qualification. Knowledge-based qualifications go beyond standard-based methods to comprehend additional sources of information into the qualification process, including information about the design, technology, and manufacturing processes. Knowledge-based qualification also should incorporate a failure mechanism-based methodology. Merits of KBQ include improvements in the method of predicting materials performance, understanding performance/reliability tradeoffs, managing risk, and using failure mechanism testing. Critical elements for KBQ development include transforming application usage conditions into stress regimens and early involvement in the process technology development. Critical concerns center on comprehending and modeling the failure mechanisms and assuring appropriate test structure to failure mechanism suppositions.

2 SCOPE AND DEFINITIONS

2.1 Part, Product, Device

In this report, the terms *part*, *product*, and/or *device* refer to silicon-based very large-scale integration (VLSI) circuits and their associated package.

2.2 Qualification

The purpose of qualifying a product for reliability is to assess its functionality in its usage environment over time. Knowledge-based or “use conditions”-based qualifications are customized procedures that rely on knowing the types of failure and application usage environments. If the method of assessment is prescribed, then the qualification process is called “stress-based” or “standards-based” and can be viewed as an assessment of the capability of a device to pass a specified set of stress test procedures [1]. The term *qualification* can also include the following:

- Verification of function and performance under specified application conditions
- Verification of the robustness of the design by simulation or reliability characterization
- Demonstration of manufacturability
- Demonstration of intrinsic reliability [2]

2.3 Stress-based Qualification

Stress-based qualifications—also known as standards-based qualifications—are documented, standardized procedures that prescribe accelerated test conditions. Prescribed conditions are usually temperature, relative humidity, duration, etc. They are typically published as an open standard or procedures document. Examples include *Stress Test Qualification for Integrated Circuits*, AEC-Q100,¹ and the *Generic Requirements for Assuring Component Reliability*; GR-357 section of the Telcordia Network Equipment Building System specification.²

¹ Automotive Electronics Council; AEC-Q100, rev. F, July 18, 2003

² Telcordia Network Equipment Building System

2.4 Applications-based Qualification or Use Conditions Qualification

Applications-based qualification or *use conditions qualification* involves procedures wherein the accelerated test conditions are determined case by case and are based on the expected environmental conditions and product usage in a defined application. Application or use conditions are usually defined by a market segment (office usage, automotive usage, etc.).

2.5 Knowledge-based Qualification

Knowledge-based qualification is a two-step process that starts with detecting and understanding failure mechanisms of a specific technology and then applying use conditions-based qualification plans based on that knowledge.

3 RELIABILITY/PERFORMANCE CHALLENGE

Producers need to ensure that the device meets its design, performance, and quality goals. The increasing complexity of technologies and products makes high confidence qualifications ever more challenging. Sustaining the industry's historic rates of IC improvements in this and future decades will require more radical changes in materials, processes, and devices, resulting in the discovery of new failure modes as well as changes in existing failure modes and mechanisms.

IC users are under pressure to build faster, better, and cheaper products. Users often want evidence to assure ICs will meet their requirements. This pressure often conflicts with expectations, large sample sizes, fixed stress requirements, extensive post-qualification monitoring, and rapid time to market.

The technologist faces tradeoffs between reliability and performance as the market pushes for higher performance found in advanced technologies. For example, increasing reliability margins can incur power penalties and enhancing performance can cut into the available reliability margin. Balancing various factors like sample sizes, fixed stress requirements, extensive post-qualification monitoring, and time to market presents significant challenges. The desired balance is to meet the users' needs in both performance and reliability.

The qualification process needs to be optimized to meet these increasing challenges. For many applications, a knowledge-based qualification will serve the IC user better than the historic stress-based qualification. Neither approach is perfect or optimal for every application. However, without improved approaches to qualification methodologies, some applications will not be able to take advantage of the performance and functionality improvements of advanced technologies. The *International Technology Roadmap for Semiconductors* [3] (ITRS) and the companion document, *Critical Reliability Challenges for the International Roadmap for Semiconductors* [4], provide a comprehensive view of future process technology and reliability.

4 STRESS-BASED QUALIFICATION

4.1 Purpose and History

A key expectation or outcome of the reliability qualification of a semiconductor product is to ensure its fitness for its intended application over the expected life of the application. Various methods and procedures have been developed to measure "fitness for use." Many consist of accelerated testing procedures that expose devices to a stringent set of environmental conditions.

The results are interpreted to infer if the parent population will survive the expected application environment and lifetime. Use of a standardized set of reliability evaluations is rooted in the approach taken by military procurement to ensure semiconductors will perform over a wide range of environmental conditions. This approach was codified in two documents: MIL-STD-883, a compilation of test methods, and MIL-M 38510, the qualification process.

The methodology developed by the military continues to be the basis for many commercial qualification procedures and methods. From a customer or user standpoint, it is a uniform approach to qualification because components from each supplier are subjected to similar tests. The approach allows components and suppliers to be easily compared. Continued use of a standardized suite of tests over time can also result in a large library of data about fail mechanisms that can be categorized and compared industry-wide. This information enhances the understanding of both the mechanisms and the performance of a given semiconductor silicon and assembly process and leads to improvements in those processes. The relative uniformity of the procedures and the historical comparative value are key strengths of the stress-based approach.

4.2 Weaknesses of the Stress-based Approach

The stress-based approach also has some weaknesses. When first introduced, reliability qualification was a reactive activity at the end of a development cycle, applying mainly standard reliability stresses as part of pre-determined general qualification plans. The product was examined as a “black box,” comparing its properties to specified requirements as a “final inspection” at the end of the product development process. The customer would often repeat the procedure with a duplicate or similar procedure. These two steps were redundant, adding another phase to development, while possibly not focusing on critical issues needing to be evaluated.

To be meaningful, reliability stresses need to accelerate the environmental conditions expected in the intended application(s). This means that the reliability stressing needed to qualify a part for use in an automobile would differ from qualifying a part for an office or data center environment. However, a review of some of the more widely employed qualification documents indicates significant similarity of the reliability qualification stresses defined even for widely varied application use conditions. An analysis of standardized qualification stress conditions required for the automotive and telecommunications segments indicates that standards-based stress criteria do not accurately reflect the expected use environment.

The traditional stress-based methods are used to test for the existence of failure modes observed in application. Thus, this method is mainly based on experience with products of mature technologies. The variable parameters of test and stress conditions are restricted to those that can be set and varied externally to the product. The parameters are usually limited to electrical and environmental operational conditions within datasheet limits. The resulting evaluation is qualitative since the relationship between applied stress test conditions and lifetime use conditions are usually not established. Therefore the value of applying stress-based methods to new or changed materials or technologies is questionable.

Failures need to be generated and understood during the process development phase, not during the formal qualification exercise. A singular application of standardized qualification stresses can also raise other issues (e.g., the supplier may invest unneeded development resources to ensure the product will “pass the test” even though the application may not require that level of performance). Additionally, reliance on passing standardized test conditions may keep the IC user from considering alternative technologies that have suitable performance.

4.3 Challenges to the Assumption of Standards-based Qualifications

Two key assumptions in the standards-based approach are as follows:

1. Semiconductor products and processes are or can be made capable of meeting the imposed requirements.
2. The prescribed qualification tests will detect all key failure mechanisms that may be experienced by the device during its lifetime.

Neither of these assumptions is completely accurate. Moore's Law continues to drive the semiconductor industry on an exponential scale [5]. Die size increases roughly 7% annually. Microprocessor transistor count has increased to tens of millions per die. Silicon-to-package interconnects have increased sixfold in the past 5 years. Power density continues to increase. New materials continue to be introduced into both silicon and package technologies [6]. The driver behind Moore's Law is performance. All markets—commercial, automotive, telecommunications, and military—demand increased performance to grow and meet their respective customers' needs. To continue meeting the challenge of Moore's Law and deliver the resultant performance, bringing new semiconductor technology to market must include evaluating the tradeoffs between reliability and performance. The industry has realized that the reliability margins of 10–15 years ago are no longer feasible. The current and projected approach is to engineer reliability and performance to ensure that reliability meets the needs of the target market with reasonable, but not excessive, margins.

As new technologies are developed, new failure mechanisms may be introduced while others disappear. Stressing must be capable of taking this into account. Few of the existing qualification specifications require stressing to failure, a determination of acceleration factors, and a subsequent decision as to the applicability of the stress conditions or criteria. However, this approach is critical as the industry moves to new processes and materials. Factors including significant cross-die temperature deltas, reduced dielectric toughness, and increased use of reliability through design make a standard set of reliability evaluations questionable.

5 KNOWLEDGE-BASED QUALIFICATION

5.1 Looking at Interrelationships Within the Product

The knowledge-based approach [7] applies a systematic procedure concentrating on the product properties and product construction to ensure capability in meeting the intended application conditions. This qualification methodology considers the relationships among design, technology, manufacturing, and product life phases at use conditions. For this approach, the customer and applications requirements have to be known with respect to

- Application conditions and durations/lifetime (use conditions profile)
- Processing/manufacturing conditions at the user
- Robustness against random external conditions (e.g., voltage pulses or temperature excursions)
- Expected statistical reliability properties (e.g., tolerable early failure rate and time period)

Applications vary based on their system requirements, application conditions, and planned time of use ranging from benign environments and short-term use to harsh environments and long-

term application. Examples include chip cards, mobile phones, consumer electronics, computers, automotive applications, and telecom networks, each with individual use or mission profiles.

5.2 Using the Failure Mechanism-based Approach

The most prominent form of KBQ, failure mechanism-based qualification, is formally described in JEDEC Standard JESD34, *Failure-Mechanism-Driven Reliability Qualification of Silicon Devices*. A detailed discussion of its application is in *Reliability Qualifications of a Smart Power Technology for High Temperature Application-based on Physics-of-Failure and Risk and Opportunity Assessment* [8].

A failure mechanism-based approach uses stress tests known or expected to address specific failure mechanisms to demonstrate the reliability performance of a technology with respect to corresponding potential failures. However, unlike stress-based qualification, a failure mechanism-based approach does not standardize either the stress set or the criteria for every technology.

Successful application of failure mechanism-based methods depends on acquiring and integrating the following:

- Reliability data
- Extrapolation models
- Application environmental conditions
- Design rules

These provide the information necessary to calculate and assess the field failure risk for a product in a specific application. The resulting decision will be a risk estimate based on known, characterized, and modeled failure mechanisms applicable to the application environment. The initiation of production or customer shipments (e.g., qualification) is then based on this risk estimate. Failure mechanism testing focuses on the robustness of the product and its production process against intrinsic failure modes, requiring small sample sizes for qualification tests and stress testing until failure to measure the failure distribution. Most stress-based tests do not fulfill these requirements.

The failure mechanism aspect of the qualification requires a physics-of-failure approach based on the following elements:

- Transformation of product requirements to the test structure level to calculate the failure condition at the test structure level.
- Data on the time dependence of the test structure parameter under different stress conditions to calculate the free parameters for a degradation model.
- A degradation model describing the time behavior of parameters (i.e., acceleration factors) with respect to stress conditions to enable extrapolation of time to fail under use conditions from the measured failure times under stress.
- Information about the correlation between special performance parameters of the product and parameters of test structures used for reliability investigations.
- A statistical model to calculate failure rates under use conditions based on stress test data.

Note that worst-case conditions have to be assumed when information about any of these elements is scarce.

5.3 Risk Management Perspective

5.3.1 Risk Management as Part of the KBQ Process

Qualifying a product or a production technology is a risk management decision based on significant statistical data. A key characteristic is the probability that the product fails under operating conditions in the application. The statistical probability of this is never zero. Thus it follows that

High Reliability Level = low risk of a failure in the field

In KBQ, understanding the reliability level needed is compared with the reliability performance data collected and the “specified requirements” (if present). Based on this, the need for additional data collection or analysis is determined. Collecting additional data to meet a specified requirement when existing data clearly demonstrates the product will perform reliably is wasteful. Resolving these types of risk questions is especially critical in situations where performance, reliability, and cost present conflicting requirements. When this occurs, several courses of action are possible:

- Ensure the stated environmental conditions represent actual and not accelerated conditions
- Ensure the appropriate failure mechanisms and models are accurate for the application
- Refine estimates of the user’s environmental conditions and acceleration factors
- Make appropriate changes in the product or technology

Risk management is the process that links the requirements with the qualification results in terms of product characteristics, reliability data, and process capability. Risk management should incorporate quality management methods such as quality functional deployment, failure modes and effects analysis (FMEA), and design of experiments. The risk management process also determines if the risk level is acceptable from the user’s and producer’s perspective and against stated requirements. The risk level assessment should be continuously updated through planning, development, and qualification processes. Based on the difference between demonstrated performance and requirements, the risk or opportunity is assessed and responses defined. The process ends when production based on an acceptable risk level begins.

5.3.2 Risk Management and Uprating

The avionics and military industries have taken another approach by applying and specifying the practice of uprating [9–10]. Many of these risk management concepts are not used when products are “uprated.” One aspect of uprating is customer testing/qualifying products to conditions outside or beyond the datasheet parameters or supplier-intended use conditions. This practice originated when technology was changing incrementally and processes provided a significant reliability margin. Testing a limited sample to “qualify” the product for an application with operating parameters outside the supplier’s intended use or operating specifications incurred some risk, mainly selecting a “qualification” sample representing a distribution at the tail rather than the center of the supplier’s process. Since products come from various sources (e.g., the distribution channel), it is difficult to determine if the material represents the main population or a tail of the supplier’s process distribution. Subsequent design and application decisions based on this “qualification data” appear to introduce an unneeded risk factor. Additionally, modifying (i.e., increasing) stress conditions or durations to “qualify” a product to an environment outside the semiconductor manufacturer’s datasheet does not ensure robustness without an in-depth

understanding of the technology and design parameters and their response to varying environmental parameters.

The impact of new processes and materials—strained silicon, copper, high- and low-k dielectrics—cannot be completely comprehended by uprating methods. “Qualifying” products intended for mission-critical applications in the avionics and military markets based on limited knowledge of the supplier’s process and performance distributions imposes significant risk and generally is not supported by the semiconductor industry. A proposed approach would be for these industries to recognize their co-dependent needs and responsibilities. Possible paths forward might include a joint effort to identify the application needs of these market segments and to develop an appropriate reliability validation and/or selection of appropriate products and technologies for the application.

6 DEVELOPING A KNOWLEDGE-BASED QUALIFICATION APPROACH

A KBQ should start by considering the application conditions. Based on these conditions, the following steps are recommended in developing a qualification plan.

- **Transform requirements based on application conditions to sub-elements of the technology and product**

Typically, customers define their requirements in terms of product performance and environmental conditions. For mass market products, requirements can often be determined from roadmaps or market requirements. In either case, the performance of a technology is specified by the performance of library cells and by the basic elements of the technology (e.g., the passive and active elements to build these cells). For example, a speed requirement for a product must be transformed to the driving capability of the minimal transistor and the maximum current per via has to be extracted to guarantee minimal cell size.

- **Select technology- and product-relevant structures for a reliability evaluation**

To evaluate basic performance with respect to reliability and manufacturability, test structures must be sensitive to the dominant known or expected failure mechanisms. Performance can be demonstrated by characterizing the library cells (including critical reliability tests). However, in the example above, applying minimum design rules to the single transistor and the via-line structure would be the most efficient and usable. Test structures that generate failure distributions within an acceptable amount of time must be chosen. It is important to generate failures, as zero failures cannot be extrapolated to meaningful models or predictions. In some cases and for some failure mechanisms, the product itself may be the optimal test structure, such as for active power cycling or specifically designed analogue design blocks.

- **Establish assessment criteria for reliability structures**

To predict reliability for a complex product based on test structure investigations, the assessment criteria of the product (i.e., in terms of lifetime at specified performance) have to be translated to assessment criteria for the test structure. This involves specifying which parametric value demonstrates product reliability. For example, characterizing I_{dsat} degradation over time should examine temperature extremes for the hot carrier mechanism and for other high temperature instabilities, such as negative temperature bias instability

(NBTI). For a via-line structure, the temperature and maximum current that produce permissible resistance degradation must be determined.

- **Define the model and stress conditions for each reliability structure to evaluate model parameters**

The information generated in the first three steps allows the test structure-based results to be extrapolated to the product. To do so, product failure mechanisms are formulated based on knowledge about the failure distributions, the test structures, anticipated use conditions and accelerated test conditions. For example, the impact of electromigration on the interconnect lines and vias could be determined using Black's formula [11]. Since a product may consist of millions of vias, the number or percentage of vias enabled during a worst-case operation mode needs to be considered to calculate the appropriate acceleration factors. Another example would be to derive hot carrier effects based on substrate current models and their appropriate probability distribution.

- **Generate reliability model parameters**

After failure mechanism-specific reliability stresses are performed, the last step is to generate the reliability model parameters to extrapolate reliability data to end of life.

7 OBSERVATIONS AND DISCUSSION ABOUT THE KBQ APPROACH

- **For every failure mechanism, a consistent and generally accepted degradation model is not available**

A characterization process before formal qualification with extreme stresses on worst-case test structures is critical to identifying and understanding new mechanisms. This process tests design rules, forces failures, and establishes failure rates for the relevant mechanisms as a function of the appropriate stresses (e.g., temperature, voltage, temperature range, relative humidity, current density, etc.). Empirical or theoretical model(s) can be fitted, and failure rates can be predicted from stress intensity, stress duration, and the functional model.

- **Because test structures typically used for KBQ are restricted to one failure mechanism, a new mechanism could be undetected**

The full set of test structures used for a qualification will normally be sensitive to more than one failure mechanisms. Stressing to failure will detect the relevant mechanisms. The strength of KBQ is that it is easier to detect a new mechanism since a deviation from the expected distribution or result indicates a new mechanism. Using test structures makes the results easier to analyze.

- **The extrapolation of results from test structure to product may not be applicable**

Properly designed test structures can offer a more definitive evaluation than the product as the test structures can be designed to explore the limits of design rules, while products often stress design rules to a lesser degree (common examples include electromigration [EM] and HCI). Extrapolation gaps can be closed by simulations that can explore beyond application ranges. Simulation beyond the application range can then be interpolated with reduced risk.

- **More knowledge is needed for a reliability evaluation with a KBQ approach than with a standards-based approach**

While a standards-based approach may seem simpler, the KBQ approach has benefits in time to market and efficient use of resources. The KBQ will produce a result that better aligns reliability performance and the customer's expectation, whereas the stress-based approach can produce only a null result (zero is pass while > 0 is fail) and no indication of the margin.

8 EXAMPLE APPLICATION OF KBQ

The failure mechanisms addressed by an example qualification plan are shown in Table 1. An efficient survey technique to detect these mechanisms is suggested. Additional tests may be required to determine the parameters for accurately modeling the mechanism.

Table 1 Guideline for Choosing Stresses for Common Failure Mechanisms

Failure Mechanism	Survey Method	Methods to Define Modeling Parameters
GOX breakdown (soft or hard)	QBD, V_{ramp}	TDDB
GOX leakage	V(BD)	TDDB
Parameter shift (V_i) caused by GOX contamination	CV, triangular voltage sweep	BTS
Device degradation (transistor, resistor, capacitor, packaging), including HCI, high temperature instability, NBTI, PBTI, interfacial charge density	IDSAT measurement	Hot Carrier Stress Bias Temperature Stress
Current density driven opens or shorts by voiding, hillocks or extrusions of interconnects or interconnect resistance change	Package level parametric test at high temp/high current	EM stress (Isothermal J,T) using test structures
Mechanical stress driven opens or shorts by voiding, hillocks or extrusions of interconnects or interconnect resistance change	Parametric/Functional Test	Stress Migration bake vs. temperature
Intermetal-dielectric-leakage	V_{ramp}	TDDB
Chip/Si fracture	Acoustic Image	Power and Temperature Cycling
Corrosion	HAST (Biased)	85/85 (Biased)
Faulty solder connection, solder fatigue	HTS, Solderability Test (steam age), TC	Wetting time, contact angle
Delamination (Inc Wire bond opens due to delamination)	JECEC Moisture Level, TC, HTS, THB, Acoustic	3- or 4-point bending, Acoustic, Decap wirepull
Wire bond opens (intermetallic driven)	Parametric/ Functional Testing	HTS (Arrhenius bake)

Note: Examples only - not intended to be comprehensive.

Table 1 suggests testing methods for the identified failure mechanisms. In some cases, depending on the material, the qualification plan may have several options. Product qualification can be based on data generated with the tests like those in Table 1, together with qualified library cells. The procedure should also include using appropriate software tools to check that the design adheres to design and reliability rules.

Stress methods targeting a broad spectrum of failure mechanisms (like high temperature operating life [HTOL]) are not needed in every case. To demonstrate the strength of other stress conditions compared to HTOL, two cases should be compared with different dominant failure mechanisms and resulting reliability data from a standard qualification specification and the proposed KBQ methods.

For a detailed example of the application of a use conditions method, see *Use Condition Based Reliability Evaluation: An Example Applied to Ball Grid Array (BGA) Packages* [13].

8.1 Example #1: Wire Bond Quality

If the dominant fail mechanism was due to effects measured by the pull strength, the acceleration factor for a 200°C test extrapolated to 150°C is only 1.6 based on an activation energy of 0.2 eV [12]. On the other hand, if Kirkendall voiding were the mechanism, this acceleration factor is 38.6, because the activation energy for this mechanism is 1.26 eV. If the temperature difference between accelerated stress and application environment or the activation energy value uncertainty is not considered, a huge uncertainty can result. This is true even when a moderate but “typical” E_a value of 0.7 eV is used to extrapolate product stress tests to the customer’s application. An activation energy value of 0.7 eV is often used if direct knowledge of the failure mechanism kinetics is unknown.

8.2 Example #2: Wafer Technology

Similar ranges for wafer technology-related failure mechanisms could be $E_a = \pm 0.1$ eV for hot carrier effects (HCE) up to 1.8 eV for surface inversion. The extrapolation of a 1000-hour HTOL test at 175°C dominated by HCE is less than 1000 hours real life at 125°C but more than 142,000 hours if surface inversion is the main failure mode.

9 CONCLUSIONS

- Advantages of KBQ include
 - Fewer parts are needed for qualification
 - Long product qualification tests are eliminated
 - The prediction of field reliability is improved, possibly lowering costs and shortening cycle time
- Limitations of KBQ include
 - Incomplete knowledge leads to incomplete reliability testing
 - The transfer of test structure results to product must be valid
 - Effectiveness of the method is only as good as the knowledge available

The strength of KBQ depends on the use of customer requirements, application and environmental conditions, failure mechanisms, and related models. Its flexible approach allows for changes in materials, process parameters, and library designs. Knowledge-based qualification is an efficient and effective way to solve the challenge of demonstrating reliability, especially for new technologies.

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