TSV: Current Product Reliability – ‘What’s Missing?’

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Package Assembly – Interfaces Well Known

- **Stacked CSP**
- **FlipStack® CSP**
- **F2F FlipStack®**
- **Logic with Embedded Memory**
- **Logic and Memory in Same Module**
- **Logic and Memory in Separate Packages**
Typical Qualification Envelope – Example

<table>
<thead>
<tr>
<th>Quality</th>
<th>Moisture Sensitivity</th>
<th>JEDEC L2 / 260°C Reflow</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Package Reliability</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Temp Cycle B</strong></td>
<td>-55°C ↔ 125°C, 1000 cycles</td>
</tr>
<tr>
<td></td>
<td><strong>High Temp Storage</strong></td>
<td>150°C / 1000 hrs</td>
</tr>
<tr>
<td></td>
<td><strong>Temp + Humidity</strong></td>
<td>85°C + 85RH / 1000 hrs</td>
</tr>
<tr>
<td></td>
<td><strong>Board Level Temp Cycle</strong></td>
<td>-40°C ↔ 125°C, 1000 cycles Failure Free</td>
</tr>
<tr>
<td></td>
<td><strong>Level 2 168 hours of 85°C / 60% RH</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Product Verification**
- 1 Lot / 22 - 77 units
  - Engineering Level

**Product Qualification**
- 3 Lots / 77 units
  - Product Level

*Non Consecutive Lots – must be from different build cycles*
Stacked CSP (SCSP) – Migration to TSV

Stacked CSP

FlipStack® CSP

F2F FlipStack®

TSV Stacked CSP
FCBGA – Migration to TSV

Logic with Embedded Memory

Logic and Memory in Same Module

Logic and Memory in Separate Packages

TSV Stacked BGA
### Qualification Envelope – 3D CSP

<table>
<thead>
<tr>
<th>Product Verification</th>
<th>1 Lot / 45 units</th>
<th>Engineering Level</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Quality</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Moisture Resistance</td>
<td>JEDEC L2 / 260C 3x Reflow</td>
<td>Pass</td>
</tr>
<tr>
<td><strong>Package Reliability</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temp Cycle</td>
<td>-55°C ↔ 125°C, 1000 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td>High Temp Storage</td>
<td>150°C / 1000 hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Temp + Humidity</td>
<td>85°C + 85RH / 1000 hrs</td>
<td>Pass</td>
</tr>
<tr>
<td>Bd Level Temp Cycle</td>
<td>-40°C ↔ 125°C, 1000 cycles</td>
<td>Not tested</td>
</tr>
</tbody>
</table>

- **45nm Node**
  - Memory ~ 100µm thick
  - Logic ~ 50µm thick with 10µm TSV at 40um pitch
  - 14x14mm Body area array bump pitch to substrate
Qualification Envelope – 2.5D BGA

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<th>Product Verification</th>
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<th>Engineering Level</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Quality</strong></td>
<td><strong>Moisture Resistance</strong></td>
<td>JEDEC L4 / 240C 3x Reflow</td>
</tr>
<tr>
<td><strong>Temp Cycle</strong></td>
<td>-55°C ⇔ 125°C, 1000 cycles</td>
<td>Pass</td>
</tr>
<tr>
<td><strong>High Temp Storage</strong></td>
<td>150°C / 1000 hrs</td>
<td>Pass</td>
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<tr>
<td><strong>Temp + Humidity</strong></td>
<td>85°C + 85RH / 1000 hrs</td>
<td>Not tested</td>
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<td><strong>Bd Level Temp Cycle</strong></td>
<td>-40°C ⇔ 125°C, 1000 cycles</td>
<td>Not tested</td>
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</tbody>
</table>

- **28nm Node**
  - Multiple Die on Interposer ; 300µm thick, 40µm µBump pitch
  - Interposer ~ 100µm thick with 10µm TSV at 210um pitch
  - 42.5x42.5mm Body with heat sink
What’s Missing?

- Reliability Testing = Good Indicator of Future Performance?
  - Many new processes and equipment = many new failure modes
  - Interaction of vertical through vias (TSV’s) with metal layers above and below the vias
  - Do we know enough about all of the new processes to know standard reliability will be a good indicator of future performance
Uncertainty at Wafer Level

• Leads to Increase in Gates & Cost
  – Added measures to protect against the unknown
    ✓ Copper Residue
    ✓ TSV Damage (liner)
    ✓ Copper Migration
    ✓ Electromigration
Wafer Finishing of TSV Devices

- Passivation and TSV Isolation
  - No Copper residue post WBG can be tolerated
  - No Damage to silicon, liner or tip can be tolerated

Silicon Etch Recess

Organic Passivation + UBM

Ni–Au on Copper Via
Liner Integrity & Cu Migration

- TSV
- Back Side Pad Metal
- Liner Intact / Un-damaged
- Damaged
Wafer Finishing of TSV Devices, cont.

• How to Verify / How Often:
  – Cu limit on Si = $2 \times 10^{15}$ atoms/cm$^3$ (Min. 20 ppb~)
  – Dynamic SIMs?
  – TOF SIMs?
  – TXRF?
Uncertainty at Assembly Level

- Again… Leads to Increase in Gates & Cost
  - Added measures to protect against the unknown

✓ Die Stacking Reliability
  - Underfill technology (voids, incomplete fill, excess fill, etc)
  - Die connectivity

  - Damage to underlying metal
Uncertainty at Assembly Level, cont.

• How to Verify / How Often:
  – Scanning acoustic microscopy (C-SAM)
  – Non-destructive technique that can be used to image the internal features of a specimen: highly sensitive to the presence of delamination sub-micron thickness (difficult to detect using X-ray radiography)
Uncertainty at Assembly Level, cont.

Known:
- Thin die warpage can cause non contact / high resistance

Unknown:
- Stress on via : liner damage
Uncertainty at Assembly Level, cont.
Uncertainty at Assembly Level, cont.
Paradigm Shift in Engineering for Reliability

- **Introduction of Loop Tracker**
  - Fab level mentality to engineering
  - Track all data and analyze for shifts
  - More cycles of learning
  - Cpk assessment earlier in development …. vs prior to production ramp
  - Much more detailed FMEA
Down Stream Risk Mitigation

- Potential Test Insertion Points
  - Vertical and Side-Side Die Stacks
Test Insertion Points

- CSP TSV Potential Test Insertion Points

F.S. Bump → B.S. Finish → Assembly Logic to Subst → Assembly Memory (Cube) to Logic → Final Test

Insert Test: Strip level O/S
Test Insertion Points, cont.

- CSP TSV Potential Test Insertion (Vertical Die Stacks)
  - Cumulative cost probably determines best test insertion point
Test Insertion Points, cont.

- Interposer TSV Potential Test Insertion Points
Test Insertion Points, cont.

- Interposer TSV Potential Test Insertion (Side-Side Die Stacks)
  - Cumulative cost probably determines best test insertion point
Summary: TSV Product Reliability

- Industry has established standards for qualification
- New processes and materials = New failure modes
- Requires extensive engineering to manage the chip package interactions
- Increased quality gates to mitigate against failure
- Cost of Quality
Thank You!