Stacked Silicon Interconnect Technology (SSIT) Qualification – Requirements and Tools

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Xilinx Inc.

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(in co-operation with Fraunhofer IZFP)
Background and Motivation
Background: FPGA

- **Building Blocks**
  - Configurable Logic Block (CLB)
    - Configuration memory
    - Programmable switches
    - Interconnect drivers
  - Hard IP (DSP, EMAC, etc.)
  - Block RAM
  - Configurable IOs
  - High-speed transceivers

Programmable SoC of logic, memory, and analog circuits
For the Most Demanding FPGA Applications

High Performance Computing

Next Gen Wired Communications

Next Gen Wireless Communications

VIRTEX®

Industry’s Highest System Performance and Capacity

Aerospace & Defense

Medical Imaging

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Introducing Stacked Silicon Interconnect Technology
High Bandwidth, Low Latency, Low Power

- Massive number of low latency, die-to-die connections
- Earlier in time
- No wasted I/O power
- Over five years of R&D

Delivers the Best of Both Worlds: High and Usable Capacity
Stacked Silicon Interconnect Technology

- Technology Overview and Requirements
- Simulation
- Failure mode Analysis
Xilinx Virtex-7 FPGA SSIT

- Low risk approach to integrate TSV & u-bump
  - Passive silicon interposer with 65nm interconnects & coarse-pitch TSV
- High density micro-bump for 10K-30K chip-to-chip connections
- Better FPGA low-k stress management with silicon interposer

**Technology** | **Specs**
--- | ---
M1-M4 | 2um pitch 4 4X layers
TSV | >10 um diameter & 210um pitch
Micro-bump | 45um pitch
C4 | 210um pitch
Package | 4-2-4 Layer, 1.0 mm BGA pitch

28nm Test Vehicle + 65 nm Interposer

*Courtesy of Xilinx, TSMC, Amkor*
<table>
<thead>
<tr>
<th>Reliability Tests</th>
<th>Focus Areas</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Level L4 Precon and TCB</td>
<td>TSV and C4</td>
<td>Passed 1000 TCB</td>
</tr>
<tr>
<td>Wafer Level TCB</td>
<td>TSV&amp; Interposer Interconnects</td>
<td>Passed 1000 TCB</td>
</tr>
<tr>
<td>Electro-migration</td>
<td>Micro-bump Joint</td>
<td>Passed 0.1% CDF for 10 years</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>Micro-bump Joint</td>
<td>Passed 1000 hours</td>
</tr>
<tr>
<td>Package Level L4 Precon and TCB – 1st Leg</td>
<td>Micro-bump Joint, TSV, C4 Interconnects</td>
<td>Passed L4 and 500 TCB</td>
</tr>
<tr>
<td>Package Technology Qualification - L4 Precon, TCB, THB, HTOL, HTS</td>
<td>Micro-bump Joint, TSV, C4, Silicon, Package</td>
<td>In progress</td>
</tr>
</tbody>
</table>
Technology Development Methodology

- **Prevention** ➔ Simulation, BKMs (Design, Process, Benchmark)

- **Failure Mode Detection** ➔ TV, FA, Accelerated Tests

- **Fix Validation** ➔ JEDEC, Use Condition Tests
## Xilinx is Well on the Way to Volume Production

### Test Vehicle

<table>
<thead>
<tr>
<th>Test Vehicle</th>
<th>CY09</th>
<th>CY10</th>
<th>CY11</th>
<th>CY12</th>
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</thead>
<tbody>
<tr>
<td>TV1 (90nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TV2 (40nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TV3 (28nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device (28nm)</td>
<td>ISE 13.1 Beta</td>
<td>TO</td>
<td>ES</td>
<td>Prod</td>
</tr>
</tbody>
</table>

### Milestones

- Module Development
- Process Integration
- Reliability Assessment
- Supply Chain Validation
- Design Enablement
- Design Validation
- Process Qualification
- EA Design Tools
- Initial Sampling

Today
Simulation DOEs to Aid Selection of Effective Material / Process Factors
## FEM Attributes and Materials

**Overall package**
- **Body size**: 42.5x42.5 mm

**Top Chip**
- **Chip size**: 4 slices, Each 7x12 mm
- **Pitch/Solder**: 45um/SnAg

**TSV Interposer**
- **Via diameter**: >10um

**Organic substrate**
- **Core thickness**: 800um
- **BGA pitch**: 1 mm
- **Interposer Pitch/bump**: 180um/Eut

### Materials Table

<table>
<thead>
<tr>
<th>Materials</th>
<th>Young’s modulus (GPa)</th>
<th>CTE (ppm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate core</td>
<td>18.9</td>
<td>x,y =11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>z =16</td>
</tr>
<tr>
<td>Si</td>
<td>150</td>
<td>3</td>
</tr>
<tr>
<td>ubump UF</td>
<td>6</td>
<td>38</td>
</tr>
<tr>
<td>C4 UF</td>
<td>8.5</td>
<td>32</td>
</tr>
<tr>
<td>Copper</td>
<td>130</td>
<td>17</td>
</tr>
<tr>
<td>Solder mask</td>
<td>2.9</td>
<td>68</td>
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<tr>
<td>Sn Ag solder</td>
<td>51</td>
<td>22.4</td>
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<tr>
<td>TIM1</td>
<td>5.8e-3</td>
<td>-</td>
</tr>
<tr>
<td>Eut solder</td>
<td>31.5</td>
<td>25.3</td>
</tr>
</tbody>
</table>
Interposer - A Stress Buffer for Active Layer

- Active Layer Stress is mitigated by Interposer
Low CTE Core – Reduces Package Stress

### Simulation DOE’s

<table>
<thead>
<tr>
<th>Leg</th>
<th>Focus point</th>
<th>Substrate material</th>
<th>C4 bump locations</th>
<th>Passivation type / thickness</th>
<th>C4 bump material</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Base structure</td>
<td>E679FGR</td>
<td>Stack</td>
<td>SiO2 / 1um</td>
<td>SnPb</td>
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<tr>
<td>2</td>
<td>Low CTE substrate material of the FCBGA</td>
<td>Sumitomo: LoZ</td>
<td>Stack</td>
<td>SiO2 / 1um</td>
<td>SnPb</td>
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<tr>
<td>3</td>
<td>C4 bump locations with respect to TSV</td>
<td>E679FGR</td>
<td>Offset / 105um</td>
<td>SiO2 / 1um</td>
<td>SnPb</td>
</tr>
<tr>
<td>4</td>
<td>Passivation type on the C4 side of the Si interposer</td>
<td>E679FGR</td>
<td>Stack</td>
<td>PI / 5um</td>
<td>SnPb</td>
</tr>
<tr>
<td>5</td>
<td>C4 bump material and dimension</td>
<td>E679FGR</td>
<td>Stack</td>
<td>SiO2 / 1um</td>
<td>Cu post / height=60um, diameter=100um</td>
</tr>
</tbody>
</table>

**C4 Bump Stress**

- **w/ UF Leg#01 vs Leg#02**
  - **8% reduction**
  - **VonMises Stress [MPa]**
    - **E679FQR Leg#01**: 789, 663
    - **LaZ Leg#02**: 726, 614

**BGA Ball Stress**

- **w/ UF Leg#01 vs Leg#02**
  - **VonMises Stress [MPa]**
    - **E679FQR Leg#01**: 315, 277
    - **LaZ Leg#02**: 301, 282

- **Low CTE Substrate reduces PKG Stress and Warpage**
Bump Fatigue After X Cycles

<table>
<thead>
<tr>
<th></th>
<th>After x cycles @ 125C</th>
<th>After x cycles @ -55C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ubump solder</td>
<td>0.12</td>
<td>0.38</td>
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<tr>
<td>inelastic strains</td>
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<tr>
<td>ubump solder</td>
<td>2.52</td>
<td>2.93</td>
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<td>inelastic energy</td>
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<tr>
<td>C4 solder</td>
<td>0.08</td>
<td>0.17</td>
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<tr>
<td>inelastic strains</td>
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</table>

Simulation: Acceptable Reliable Fatigue
Failure Mode Analysis – Standard Tools are Effective
Top view of the Package and Die
**Open Failure Analysis**

- Electrical failure isolation is challenging – but feasible!
  - Assembly vendors need to stretch capability for process improvement feedback
Cross Section of the Open Micro-bump

The left image is the X-ray of the final cut of the open micro bump and the right image is the SEM overview of the open micro bump.
EDX Analysis of Open Micro-bump

Contamination is root cause of open micro-bump

- Combination of Tools, Process, Layout is key for Effective Failure Analysis
Xilinx leads industry with Stacked Silicon Interconnect technology delivering breakthrough capacity, bandwidth and power efficiency.

Stacked Silicon Interconnect Technology
- 2X FPGA capacity advantage at each process node
- Core part of Virtex-7 family
- Supported by standard design flows