Residual Silicon Thickness Mapping using a High Throughput Defect Inspection System for Advanced 3D IC Packaging

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Nanometrics, Inc, SEMATECH, Fogale nanotech
Outline

- SPARK API Technology
- Residual Silicon Thickness (RST) Measurement Technique
- RST Use Case - Measurement Results (Ongoing Work)
- Conclusions
Outline

■ SPARK API Technology
SPARK: Fab Wide Applications

SPARK: Advanced Macro Inspection

Advanced Package

Patterning

Transistor

Interconnect

CMP/CVD

Advanced Materials

NANOCD Suite

NANOFIBRE

NANOSTATION

NANOMET

NANOMATCH

ETCH

LITHO

UniFire

SPARK

FILL

CLEAN

PLATING

CLEAN

UniFire

Atlas XPS

Lynx

Atlas XP

CMP Residues

Bonding & Grinding Faults

Processing Uniformity

Scanner & Track Errors

Predictive Metrics for a Nano World
Advanced Wafer Packaging Integration:

- TSV Formation
- Cu pillars Formation
- Wafer to Carrier Bonding
- Wafer Thinning
- Backside TSV Reveal Passivation
- µBump
- De-Bonding
- 3D Stacking

**SPARK**
- Backside processing
- De-bonding
- Edge trim, glue dispense
- Temporary bonding integrity
- Post-thinning inspection
- De-bonding residuals
Key features for bonded wafers inspection

- Full wafer inspection in seconds
- Dual channel: Scattered and reflected light imaging
- Large depth of focus → inspect up to 2mm substrate thickness w/o auto-focus
- Multiple wavelengths darkfield → Tunable penetration depth
- Carrier, Adhesive and Glue inspection
MRM module

- MRM integrated on EFEM, with full automation connection to SPARK

- Equipped with
  - IR-Visible camera
  - Dual IR-interferometry (IR-OCT)
  - IR review in transmission mode
  - Visible review in reflection mode

- Applications
  - Multi-layers stack, Thickness, Bow/Warp, TTV
  - Residual silicon thickness (0 to 775µm)
  - Edge Trimming, Edge chipping monitoring
  - Review of surface and buried defects
**Combination of Unique Capabilities for 3D integration**

**Post-Grinding:**
- BF inspection of dimples, grinding topography, chipping & edge

**Post-Grinding:**
- DF inspection of residual silicon thickness & exposed Cu vias

**Post-Bonding:**
- NIR Inspection of voids, delamination & embedded particles

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**SPARK**
- Dimples
- Exposed Cu nails

**MRM**
- Bow/Warp
- Glue Layer TTV

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**SPARK API – Single platform to address advanced packaging**
Outline

- Residual Silicon Thickness (RST) Measurement Technique
RST measurement in the process flow

- SPARK API provides RST measurements Post-Thinning
- RST measurements will help predict TSV reveal and fine tune grinding process

- Measuring > 80 Wafers/Hour
- Measuring >80 Wafers/Hour
Spark API – RST monitoring concept

- SPARK-API consists of fast, one-shot full wafer inspection
- MRM to perform point-focused IR-interferometric thickness metrology
- MRM is used to measure RST over a few individual Cu vias => calibration of SPARK inspection data

Full wafer imaging with SPARK @ multiple wavelengths

Point-focused IR interferometry with MRM for reference data

Full wafer RST monitoring with correlation

RST ~ 5um

RST ~ 0um
RST Automated Measurement Technique

Image Collection
• Obtain Full Wafer Dark Field Images using Multiple Colors/Wavelength
  • 1st wavelength – DF VIS - limited penetration depth => to get surface information
  • 2nd wavelength – DF NIR - penetration depth to match the target RST value => surface and bulk information

Image Analysis
• DF illumination sees Cu nails below the surface
  • Intensity of the light scattered from the Cu nails is inversely correlated to the RST (higher intensity => lower RST)

Image Processing
• Image processing to bring out the bulk information
  • Divide the NIR from the VIS Image => bulk RST information
  • Remove Grinding marks => with Cu-nails signal

RST Data Extraction
• Reference Data Measurement using MRM
  • Build Correlation curve => Calibrate SPARK

Process Control
• Feed Forward & Feedback Loop
  • Feed backward to grinder => optimization of next wafer thinning
  • Feed forward to recess etch => compensate grinder profile

Has to be performed only once per device type
**SPARK – RST sensitivity**

- Buried copper nails will scatter DF light
- DF scattered intensity inversely related to RST
- DF wavelength is selected to match RST range

→ High Scattering = Thin RST
→ Low scattering = Thicker RST
Outline

- RST Use Case - Measurement Results
## SEMATECH Wafers summary

<table>
<thead>
<tr>
<th>Slot</th>
<th>Process group</th>
<th>Note</th>
<th>Full wafer image</th>
<th>Center</th>
<th>Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td>3, 6, 7, 8, 9, 10, 11, 13, 14</td>
<td>Normal</td>
<td>Surface contamination, Center with thinner RST</td>
<td><img src="image1.png" alt="Full wafer image" /> <img src="image2.png" alt="Center" /> <img src="image3.png" alt="Edge" /></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Small Excursion</td>
<td>Surface contamination, Exposed copper nails @ center (small area)</td>
<td><img src="image4.png" alt="Full wafer image" /> <img src="image5.png" alt="Center" /> <img src="image6.png" alt="Edge" /></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Large excursion</td>
<td>Exposed copper nails – Large area wafer edge and center</td>
<td><img src="image7.png" alt="Full wafer image" /> <img src="image8.png" alt="Center" /> <img src="image9.png" alt="Edge" /></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15, 16</td>
<td>Deeper RST</td>
<td>Heavy surface contamination, TSVs not visible</td>
<td><img src="image10.png" alt="Full wafer image" /> <img src="image11.png" alt="Center" /> <img src="image12.png" alt="Edge" /></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Multi-wavelengths \(\rightarrow\) Sensitivity optimization

- SPARK DF channel \(\rightarrow\) Can illuminate the wafer at different wavelengths
- Normalized image \(\rightarrow\) Keep information from Copper nails only
- Normalized image \(\rightarrow\) Used for correlation to reference data
SPARK Full wafer imaging

- Multi-wavelength capabilities provide post-thinning full wafer monitoring at high throughput
Within-Die Intensity variations

- For zones of similar TSV densities, DF intensity variations provide within-die RST variations information.
SPARK DF – Correlation to Reference Data

- Reference data collected within wafer, for
- Correlation curve saved in recipe
- Spark output → Color map indicating RST excursions

![Graph showing typical correlation with equation: 
\[ y = -3.107 \ln(x) + 33.462 \]
\[ R^2 = 0.9244 \]

Reference data [µm] vs. SPARK INTENSITY [a.u.]

Area of interest

Color map
Sensitivity To Varying RST

Median RST 8 um

Median RST 6.7 um

Median RST 4.3 um

Median RST 2 um

In Spec

Excursion

RST Thinning – Increasing Copper Nail Exposure
Typical KLARF – Automated Data Transfer to Host

RST Cut-off is 4 microns

KLARF empty if RST less than 4 Microns

Slight Excursion

Large Excursion

Slot 8

Slot 12
**RST Process Control**

- Spark detected large Wafer-to-Wafer & within-wafer RST variations
- Pre-Thinning: RST - MRM to measure RST > 20um

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Feedback to Grinder  
Feed-forward to Etch

Pre-Thinning RST check with MRM  
Rough/Fine Grinding  
Post-Thinning RST Inspection  
Backside TSV Reveal Passivation  
Post-Reveal inspection
Conclusions

- This data is work in progress and we have seen good sensitivity to varying RSTs both within wafer & wafer to wafer
- SPARK provides One-Shot Map of the entire RST variation and process excursion
- With the SPARK tool placed between the Process Grind & the TSV Reveal Step, both Feed-forward & Feedback mechanism can be employed for process control