Metallization Opportunities and Challenges for Future Back-End-of-the-Line Technology


October 5-7, 2010
Outline

- **Introduction**
  - Innovation and Copper Damascene Extendibility

- **Damascene Fill**
  - Extendibility of electroplated Copper

- **Electromigration and Stress Migration**
  - Microstructure, alloys and cap layers

- **Time Dependant Dielectric Breakdown**
  - Damascene profile

- **Resistivity**
  - Barrier layer volume
  - Alternate metallurgy
Scaling (Miniaturization):
- Moore’s Law: Circuit density
- Dennard Scaling: CMOS performance

"Scaling by Innovation" is increasingly required to stay on the path
Conventional Damascene Copper Extendibility?

**Barrier Layer(s)**
- TaN/Ta, AlOx, MnOx, other

**Seed Layer(s)**
- PVD Cu, CVD/ALD Co, CVD/ALD Ru, other

**Fill Metallurgy**
- Plated Cu, CVD/ALD Cu, PVD Cu, other

---

Poor Damascusne Fill: Multitude of Causes

Poor Fill Leads to Voiding (Hollow Metal)

- Full width
- Slit/Side void
- Center void
- Corrosion

Reasons for Poor Fill

- Profile shape (re-entrant)
- Barrier contamination (oxygen)
- Cu seed coverage (non-conformal or agglomerated)
- Electroplated fill (poor “superfill”)
- Polish (corrosion)
Extendibility of Electroplated Copper Fill

Unique NiSi Trench Structures

Plated Cu Fill of NiSi Trench Structures

Plated copper fill at 10 nm opening with an aspect ratio of six.
Electromigration Degradation and Scaling

**EM Lifetime Degradation with Scaling**

- Copper surface to volume ratio increasing, number of atoms on fastest diffusion path increasing
- Copper volume decreasing, fatal void volume smaller, shorter time to failure
- Increasing polycrystalline copper volumes, additional fast grain boundary diffusion paths
- $J_{use}$ drops by approximately half for each new generation

*C.-K. Hu et al., IEEE-IRPS Proceedings, 222 (2004)*
Electromigration Resistance Extendibility

**EM Lifetime Improvement**

- Stopping or slowing grain boundary diffusion by bamboo/blocking microstructure or by adding alloy elements to grain boundaries

- Stopping or slowing surface/interface diffusion by choice of appropriate interface or cap materials or the segregation of alloying element

---

C.-K. Hu et al., AIP, “12th International Workshop on Stress-Induced Phenomena in Metallization”, (2010), in press
Time Dependant Dielectric Breakdown Degradation and Scaling

**TDDB Degradation with Scaling**

- Higher density, smaller pitches, degradation of tolerances
- Lack of voltage scaling, higher electric fields
- Lower k dielectrics, higher susceptibility to defects, lower break down voltages
- Processing (polish, pre-cleans, RIE) damaged top of dielectric layer
TDDB: Dielectric Constant vs. Spacing Trade-Off

**TDDB Enhancement**

- Reduce propensity of damage during polish, RIE and pre-cleans
- Decrease line edge roughness
- Limit moisture and oxygen uptake in low-k dielectric
- Trade-off between dielectric constant and pitch/interconnect spacing
Resistivity Increase and Scaling

Increasing Resistivity with Scaling

- Interconnect dimensions falling below the copper electron mean free path (39 nm)
- Barrier and secondary seed layers occupying a greater volume percent
- Line edge roughness increasing as a percentage of line width
- Smaller polycrystalline grains
- Alloying for EM and SM

Model: Mayadas/Shatzkes combined with Fuchs/Sondheimer using the Mattiessan rule (Physical Review B 81, 155454 (2010))

\[ \rho_{\text{bulk}} = 1.7 \ \mu\Omega\cdot\text{cm}, \ \text{Aspect Ratio} = 2, \ R = 0.43 \text{ and } P = 0.52 \]
Extendibility of Copper Diffusion Barriers

100 nm Cu / poly-Si

100 nm Cu / 1 nm TaN / Si(100)

100 nm Cu / X nm TaN / Si(100)

TaN Copper Diffusion Barrier Robust at 1 nm in Thickness
Alternate Metallurgy: Better Electromigration and Resistivity Scaling

**Advantages**

- Smaller electron mean free path (Mo, W, Ru around 10 nm)
- Higher melting points, (Mo – 2.4x, W – 3.1x and Ru – 2.3x), lower diffusivity, higher electromigration and stress migration resistance

**Trade-off**

- Higher bulk resistivity (Mo – 3.1x, W – 2.8x and Ru – 4.4x)
Subtractive Etch Alternate Fabrication: Benefits and Challenges

**Benefits**

- Larger aspect ratio, lower resistance
- Conformal metal seed layer not required
- No dielectric RIE, eliminates damage, improve TDDB
- Dielectric collapse not an issue

**Challenges**

- Line edge roughness
- Dielectric gap fill
- Dielectric CMP
Resistivity Comparison: Copper and Tungsten Interconnects

Copper and Tungsten Fine Lines

<table>
<thead>
<tr>
<th>Resistivity (µΩ-cm)</th>
<th>Cross Sectional Area (nm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>1000</td>
</tr>
<tr>
<td>8</td>
<td>2000</td>
</tr>
<tr>
<td>10</td>
<td>3000</td>
</tr>
<tr>
<td>12</td>
<td>4000</td>
</tr>
<tr>
<td>14</td>
<td>5000</td>
</tr>
</tbody>
</table>

75-90 nm Sputtered Tungsten Blanket Films

- Tool 2: As-Dep. Beta Phase
- Tool 2: As-Dep. Alpha Phase
- Tool 1: Compressive Stress
- Tool 1: Near Zero Stress
- Tool 1: Tensile Stress

Decreasing W Resistivity

- Phase, alpha
- Stress, near zero
- Underlayer, SiO₂ lowest
- RIE processes, contamination
Conclusions

- Copper damascene metallization is likely extendible beyond the 30 nm linewidth (1800 nm² area) nodes. For obtaining void free fill and adequate reliability there will be trade-offs, namely higher resistivity.

- Other metallurgy and fabrication schemes will start to be considered as the sub-20 nm linewidth (800 nm² area) nodes are reached. Higher melting points (better electromigration resistance), lower electron mean free paths (less scattering) and resistivities closer to that of copper alloys, will become attractive.
Acknowledgements

R. Achanta       J. Kelly
G. Biery         D. Klaus
G. Bonilla       C. Lavoie
R. Bruce         Q. Lin
J. Bucchignano   E. Liniger
J. Emans         F. Liu
S. Engelmann     M. Lofaro
M. Frank         V. McGahay
N. Fuller        T. Nogami
L. Gignac        W. Price
M. Guillorn      T. Shaw
E. Joseph        T. Spooner

-- Staff of the IBM Watson Microelectronics Research Laboratory
-- This work was performed by research alliance teams at various IBM research and
development facilities
-- Research at the National Synchrotron Light Source, Brookhaven National Laboratory
is supported by the U.S. Department of Energy, Contract No. DE-AC02-98CH10886