Low k (k=3.0)/Cu Dual Damascene Process for Sub-40nm DRAM

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## DRAM BEOL vs. Logic BEOL

### More Difficult Structure

<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual damascene A/R</td>
<td>&gt; 4.0</td>
<td>&lt; 3.0</td>
</tr>
<tr>
<td>Low-k application</td>
<td>Global metal</td>
<td>Intermediate metal</td>
</tr>
<tr>
<td>Crack-stop layer</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Fusing method</td>
<td>Laser blowing</td>
<td>Electrical</td>
</tr>
</tbody>
</table>

### Speed Critical Layer!

*vs.*

Mechanically Vulnerable to Harsh Package Processes

### Chip Size Consideration!

*vs.*

Crack Propagation into Main Chip

### Thermal Expansion Difference

Adhesion, Modulus/Hardness

- Forget about Low-k! Simply Add a Metal! :)
- Even though, it is More Expensive! :(  

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For conventional 2Cu + 1Al pad DRAM, only 1 intermediate and 1 global metal under passivation.

※ Arbitrary scale
Still, no DRAM chip makers use Low-k IMD for their major products. Why?

- Hesitation in Adopting Low-k to DRAM BEOL

- Adding a metal instead of Low-k adoption
  → Low-k reliability issue
Test Vehicle (sub-40nm)

- Comparison of Conventional 2Cu +1Al pad /w TEOS and /w Low-k V1/M2 IMD

Electrical properties, Reliability, Packaging Issues
TEM of Test Structure

✓ Low-k IMD & SiCN DB @ V1/M2
VFDD process scheme

※ VFDD (Via First Dual Damascene)

① Via photo
② Via etch
③ Via fill
④ Oxide HM
⑤ Trench photo
⑥ Trench etch
⑦ Via filler ashing
⑧ SiCN open
⑨ clean/PVD/EP
⑩ CMP

✓ Conventional VFDD processes
## Low-k & Integration processes

<table>
<thead>
<tr>
<th></th>
<th>Deposition Method</th>
<th>PECVD</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Low-k IMD</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deposition Chemistry</td>
<td>Siloxane based precursor / Oxygen ambient</td>
<td></td>
</tr>
<tr>
<td>Pristine k</td>
<td>3.0</td>
<td></td>
</tr>
<tr>
<td><strong>SiCN ESL/DB</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deposition Method</td>
<td>PECVD</td>
<td></td>
</tr>
<tr>
<td>Deposition Chemistry</td>
<td>Silane based precursor / Ammonia ambient</td>
<td></td>
</tr>
<tr>
<td>Pristine k</td>
<td>5.0</td>
<td></td>
</tr>
<tr>
<td>Pre-treatment</td>
<td>Ammonia ambient plasma</td>
<td></td>
</tr>
<tr>
<td><strong>Integration</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design rule</td>
<td>&lt; 40nm (Gate size)</td>
<td></td>
</tr>
<tr>
<td>Scheme</td>
<td>VFDD</td>
<td></td>
</tr>
<tr>
<td>Etching</td>
<td>Fluorocarbon / Oxygen based ambient</td>
<td></td>
</tr>
<tr>
<td>Ashing</td>
<td>Oxygen based ambient</td>
<td></td>
</tr>
<tr>
<td>Wet Cleaning</td>
<td>Diluted Hydrofluorine acid</td>
<td></td>
</tr>
<tr>
<td>Cu BM</td>
<td>Ta based PVD</td>
<td></td>
</tr>
<tr>
<td>EP Cu</td>
<td>Pure Cu</td>
<td></td>
</tr>
<tr>
<td>Cu CMP</td>
<td>Same as SiO$_2$ IMD</td>
<td></td>
</tr>
</tbody>
</table>

✓ Conventional VFDD processes for Low-k IMD & SiCN DB @ V1/M2
Electrical properties

✓ Via-1 Rc

✓ Metal-2 Rs

✓ Metal-2 Leakage

✓ Metal-2 EM Reliability

✓ No difference of Via-1 Rc, Metal-2 Rs, Metal-2 Leakage and EM Reliability
Effective-k of Low-k IMD after Integration

✓ Computational Simulation with the Pattern Dimensions by TEM

✓ M2 Effective-k = 3.14 (Pristine k = 3.0)

✓ < 5% Increase (Robust Enough to be Compatible with the Conventional DRAM BEOL)
Packaging: Laser Fusing

Successful Laser Fusing with Modified Scheme @ Low-k/Cu Fuse

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (ppm/°C)</th>
<th>Relative adhesion energy with low-k (a.u.) @ 4pts bending technique</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-k</td>
<td>14 *</td>
<td>-</td>
</tr>
<tr>
<td>SiCN</td>
<td>3.9 *</td>
<td>2.5</td>
</tr>
<tr>
<td>SiN</td>
<td>1.5 *</td>
<td>1.0</td>
</tr>
<tr>
<td>Cu</td>
<td>16 *</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Packaging : Sawing

✓ Top view

✓ Vertical view

PSPI edge

Main chip  Scribe lane

✓ No encroachment into PSPI edge
✓ No severe chipping
With Optimized NH3 plasma pre-treatment, No delamination was observed during Bond Pull Test.

Delamination @ M2 SiCN DB and Low-k IMD interface → Due to the low interfacial adhesion energy
Conclusion

- Tough environment for Low-k Adoption into DRAM BEOL compared to Logic BEOL

- Low-k/Cu Dual Damascene Evaluation with Conventional DRAM BEOL

- **Electrically No Difference**
  (Via-1 Rc, Metal-2 Rs, Metal-2 Leakage and EM Reliability)

- **Effective-k of Low-k IMD < 5% Increase**
  (Robust enough to be compatible with the conventional DRAM BEOL)

- **Compatible with Conventional DRAM Packaging**
  (Laser Fusing, Sawing and Wire Bonding)

- **Promising Candidate** for the Next Generation DRAM Interconnection

- Further Study on Integration and Package is Required