Thermo-Mechanical Reliability of Through-Silicon Vias (TSVs)

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- Freescale Semiconductor: John Dixon, Varughese Mathew
- Global Foundries: Kamal Karimananal
- Intel Corp.: Sriram Muthukumar
- Texas Instruments: Margaret Simmons-Matthews, Yaoyu Pang, Kurt Wachtler
Outline

• Why TSV?
• TSV Fabrication
• Thermo-Mechanical Reliability Modeling and Results
• Summary
Motivation for 3D ICs with TSVs

• Motivation: Vertically integrate and connect semiconductor strata to combine similar or hybrid technologies to gain:
  • Reduced interconnect latency
  • Reduced interconnect power consumption
  • Increased bandwidth
  • Reduced form factor
  • Integration of differentiated technologies
  • Yield improvement (compared to SoC)
1. Thin substrate to ~300um

2. Pattern and etch TSV holes

3. SiO₂ formation

4. Seed layer formation
5. Seed repair (Cu electroless)
6. TSV filling
7. Cu burden thinning down

8. Dry film double-patterning

9. Cu/Ti etching
10. PR removal
Mask Layout

28 Coupons per wafer
# TSV Daisy Chain Design

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Circular Vias – Lithography Results

Design 1

| Circle (C4) | 65 | 30 | 30 | 155 |
## Square Vias – Lithography Results

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Annular Vias – Lithography Results

Design 1

| Annular (A) | 25 | 65 | 20 | 30 | 30 | 155 |
Through Via Filling

- Void Free Filling.
- 10 um Cu overburden on Top and Bottom of Substrate.
- Plated as Through Via.
- No handle Substrate.
- Next Step: Etch Cu on Either Side.
Results – Pad Layer Etch

Pad Formation

38um

12um

22um

160um
Simulation Outline

• 2D Fracture Analysis
• 3D Analysis
  – Cu Pumping and Sinking
  – Different TSV Geometries
  – Fabrication-Induced Defects
  – TSV in a Package
# Material Models

<table>
<thead>
<tr>
<th></th>
<th>Cu</th>
<th>SiO₂</th>
<th>Si</th>
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<tbody>
<tr>
<td>Young’s Modulus (GPa)</td>
<td>Table below</td>
<td>71.4</td>
<td>130.91</td>
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<tr>
<td>Poisson ratio</td>
<td>0.3</td>
<td>0.16</td>
<td>0.28</td>
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<tr>
<td>CTE (ppm/℃)</td>
<td>17.3</td>
<td>0.5</td>
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<table>
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<th>Temperature (℃)</th>
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<th>95</th>
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<tbody>
<tr>
<td>Young’s Modulus (GPa)</td>
<td>121.00</td>
<td>120.48</td>
<td>117.88</td>
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<tr>
<td>Temperature (℃)</td>
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<tr>
<td>Young’s Modulus (GPa)</td>
<td>115.24</td>
<td>112.64</td>
<td>110.00</td>
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<td>Temperature (℃)</td>
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<tr>
<td>Plastic Curve</td>
<td></td>
<td></td>
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<tr>
<td>- stress (MPa) vs. strain</td>
<td>121@ 0.001ε</td>
<td>186@ 0.004ε</td>
<td>217@ 0.01ε</td>
</tr>
<tr>
<td></td>
<td>234@ 0.02ε</td>
<td>248@ 0.04ε</td>
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Stress and Fracture Analysis

- Axisymmetric model
- Isothermally loaded with the stress free temperature to be 50 C, which was got from XRD measurement
- Large shear stress exist near the corners
Equivalent plastic strain through via at 300°C

- Cu via yielded near the corners
Fracture modeling

- Assumptions
  - Linear elastic fracture
  - Only one crack (cohesive/interfacial) exists in the TSV at a time; Cohesive crack grows along 45 degrees
  - Contact elements to avoid penetration
  - Energy release rate $G$, got by forward finite difference

Note: notation $T$ represents through-via; $B$ represents blind-via; $C$ represents cohesive crack; $I$ represents interfacial crack.
Energy Release Rate of interfacial crack in Through-via

- Interfacial crack TI-3 is critical in Through-via
- Open crack in one temperature extreme will close on another temperature extreme
  Note: red arrows indicate OPEN cracks; white ones indicate CLOSE cracks
- Cohesive crack TC-3 is the critical in Through-via.
- Although the G value of TC-1 is the largest, cohesive crack is unlikely initiate from here, because the high $G_c$ value of Cu.
Crack length vs. G value at TI-3

- At TI-3 in Through-via, as crack grows, G keep increasing, results in unstable crack propagation
- Other critical location shows unstable crack propagation
### TSV designs and dimensions

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- Above tables show the dimensions of different TSV designs, which will be analyzed and compared in the following FEM analysis.
Circular vias

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- 1/8 models were built
- Ramp temperature from stress free (50°C) to 125°C
- Design C4 was used to compare with other designs and study the effect of voids and undercutting
Cu “pumping” at 125°C

- Cu “pumping” occurs at high temperature (125°C)
- At 125°C, expansion of Cu via is constrained by Si wafer, causing large compression stress at Cu via center and tensile stress in the Si/SiO₂
- The differential expansion of Si and Cu via may cause large stress near Cu/SiO₂ interface
Cu “sinking” at -40°C

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- Cu “sinking” occurs at low temperature (-40°C)
- At -40°C, shrinkage of Cu via is constrained by Si wafer, causing large tensile stress at Cu via center and compression stress in the Si/SiO₂
- The differential expansion of Si and Cu via may cause large stress near Cu/SiO₂ interface
Effect of temperature range (cont.)

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Equivalent plastic strain in Cu via

- The plastic strain distribution in Cu is close, indicating the same critical locations (Via upper corner)
- Higher temperature results in much larger plastic strain in Cu
Using 2D (axial symmetric) and 3D models to analyze circular via (C4)
Both 2D and 3D give similar axial displacement distribution. The magnitude difference is also small, within 10%
2D vs. 3D model (125°C)

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- Both 2D and 3D give similar von Mises distribution. The magnitude difference is also small, within 11%.
- **2D model can only analyze axial symmetric via (circular-via) with circular pads.**
### Annular via

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- 1/8\textsuperscript{th} models were built
- Ramp temperature from stress free (50 °C) to 125 °C
• 1/8th models were built
• Ramp temperature from stress free (50 °C) to 125 °C
Different Via Shapes – Dielectric Stress at 125°C

- For vias with the same pitch but different shape, the annular via has smallest stress in dielectric layer.
- Square via has the highest stress and plastic strain and more likely to crack dielectric layer and Cu core.
Electroplating and Voids

• Although Cu electroplating is well established process used for TSV filling, void-free filling is still a challenge, especially for fast filling and high aspect ratio TSV filling.

• To analyze how those voids will affect the TSV reliability, single elliptical void or randomly generated spherical voids were created within the Cu core.
Circular via with single void

Zhi-Wen Sun, Girish Dixit, Optimized bath control for void-free copper deposition, Solid State Technology

- 1/8th models were built
- An elliptical void (40um×12um) was modeled in the Cu via to simulate what was observed in actual TSV sample
- Ramp temperature from stress free (50 °C) to 125 °C
The elliptical void increases the maximum equivalent plastic strain in the Cu.

Large plastic strain also occurs near the void surface, creating potential fracture initiation spot.

**Equivalent plastic strain at 125 °C**

- **Plastic strain in Cu via (circular via C4)**

![Graph showing equivalent plastic strain](image)
The void does not obviously change the 1st principal stress distribution in the dielectric layer.

The existence of void alleviates the stress in the dielectric layer, but the change is limited.
Circular via with voids

Pradeep Dixit and Jianmin Miao, Aspect-Ratio-Dependent Copper Electrodeposition Technique for Very High Aspect-Ratio Through-Hole Plating

- 1/8th models were built
- Random distributed sphere voids in Cu were modeled
- Ramp temperature from stress free (50°C) to 125°C
Effect of void percentage (Circular via at 125°C)

- Fix void radius as 3um, change void volume percentage. For each percentage, five cases were analyzed.
- 1st principal stress in dielectric layer top corner generally decreases when voids occur (compare to no void case), with large scatter as void percentage is low (1%).
- MAX plastic strain in Cu vias increases as void percentage increases.
Design parameter effects

- Both plastic strain in Cu & principal stress in SiO₂ increase with larger diameter
- The existence of voids decreases the stress SiO₂, however, increases the plastic strain in Cu
- The effect of wafer thickness and pitch on the stress/strain is small
Cu via fatigue life prediction

- Plastic strain accumulated in each cycle stabilized after 12 cycles, being about 0.00703, therefore, strain range is 0.003515
- Base on previous Coffin-Manson type equation, fatigue life of Cu via is more than 2700 cycles
Global model-Displacement $U_y (@ -40^\circ C)$

- Global warpage dominates

![Diagram showing global warpage and displacement $U_y$](image)
Global-Sub model (@-40°C)

- Inter-Chip bumps are more critical than in the TSV region
Solder and Cu pillar near the solder interface experience high strains, especially near the solder/Cu interfaces.
TSV in a Package vs. in a Free-Standing Wafer (Uy @ -40°C)

- The Uy of TSV in package is contributed from:
  - Global deformation due to warpage (results from global thermal mismatch)
  - Deformation due to local thermal mismatch
- Global effect dominates
TSV in a Package vs. in a Free-Standing Wafer (Interfacial shear @-40°C)

- The shear stress contours as well as shear stress magnitude are roughly the same for the package case and the free-standing case.
- In both cases, the maximum shear stress occurs near the edges of TSV/SiO₂ interface.
TSV in a Package
vs. in a Free-Standing Wafer (Radial stress @-40°C)

- Tensile opening stress at the interface as illustrated for the free-standing wafer case. Therefore, interfacial delamination in TSVs is a concern in free-standing wafers;
- The radial stress near the Cu/SiO₂ interface of TSV in the package is compressive due to the presence of other components in the package. Thus, it may not be a concern when TSVs are in a packaging configuration.
Higher strains occur in Cu pillar that are bonded to solder material in the packaging configuration compared to the unconstrained Cu pillar in a free-standing wafer, and thus the critical location has shifted to the microbump region for a packaging configuration.
TSV location effect (@-40°C)

- TSVs/bumps near the corners and edges of TSV array have larger stress/strain
Summary

• Cu pumping/sinking is a concern with Cu burden
• Annular and circular vias are preferable over square vias
• In the selected design parameter range, the effect of wafer thickness and pitch on the stress/strain is small
• Voids in Cu help against dielectric cracking; however, Cu cracking will be a concern
• In 3D package, global thermal/loading effect dominates overall displacement
• In 3D package, microbumps are more critical than TSVs
• Experimental validation of the failure mechanisms will be carried out