Reliability of 3D IC with Via-Middle TSV: Characterization and Modeling

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Motivation: Build Reliable 3D IC Technology

From product idea...

...to integrated prototype

Mobile wide IO on logic

~1k TSV

1-2 layers DRAM

FCBGA substrate

Logic die

LOGIC

DRAM

Backside Polymer isolation

Backside RDL and Cu µbump

SnAg

Cu µbump

Cu µbump

SnAg

Backside RDL and Cu µbump

LOGIC

TSV

DRAM
3D-Reliability Domains

- TSV
- TSV and its environment
- Stacking
- Chip Package Interaction
- Backside Processing
3D-Reliability Domains

- TSV
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3D IC Reliability Workshop
TSV Process Flow

via etch

oxide liner

barrier seed

Cu ECD Fill

TSV anneal & CMP

5µm
Cu Chemistry Impact on Cu Stress

3 Cu chemistries were studied: A, B, and C

Chemistry A

Chemistry B

Chemistry C
- shows 3 times higher stress
- exhibits more elastic response
Cu Chemistry Impact on Cu Grains

- **Chemistry A**
  - As deposited Cu film
  - After sintering temperature cycling
  - Grain growth
  - 50um

- **Chemistry B**
  - As deposited Cu film
  - After sintering temperature cycling
  - Grain growth

- **Chemistry C**
  - As deposited Cu film
  - After sintering temperature cycling
  - No significant grain growth
Annealing Impact on Cu Properties

- To understand the evolution of the material response of Cu-TSV w.r.t. the applied thermal treatment.
- Test performed by nano-indentation

<table>
<thead>
<tr>
<th>Test #</th>
<th>Sample Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>As-deposited: no aging/no annealing</td>
</tr>
<tr>
<td>2</td>
<td>Room temperature aging: 6 months</td>
</tr>
<tr>
<td>3</td>
<td>Annealed: 420° C (20 min) + 300° C (15 min)</td>
</tr>
</tbody>
</table>
Cu Properties Evolution

Nano-Indentation

Top

Bottom

Relative Position (μm)

Hardness (GPa)

As-Deposited
RT Aged: 6 Months
Annealed: 420C+300C

Overburden

Top

Bottom

Relative Position (μm)

E-Modulus (GPa)

As-Deposited
RT Aged: 6 Months
Annealed: 420C+300C

Overburden

Top

Bottom

FIB

EBSD
Control of Copper Pumping

Unoptimized thermal treatment

Optimized thermal treatment

Model

Does the pumping damage barrier oxide and brings charges/traps there?
3D IC Reliability Workshop

**TSV Parasitic Capacitance**

- **Interface trapped Charges ($Q_{it}$):**
  - Exist at the Si-SiO$_2$ interface
  - Negative interface states cause undesired C-V shift

- **Fixed Oxide Charges ($Q_f$):**
  - Exist near the Si-SiO$_2$ interface
  - Positive fixed oxide charges cause desired C-V shift

- **Oxide Trapped Charges:**
  - May exist in the entire oxide
  - Positive trapped oxide charges cause desired C-V shift
  - Negative trapped oxide charges cause undesired C-V shift

- **Mobile Ionic Charge ($Q_m$):**
  - Undesirable

**Effect of Interface states on MOS C-V**

... Can we control the oxide charges reliably?
... Is the method repeatable and reliable?

Source: “Physics of Semiconductor Devices” by S. M. Sze
Thermo-Cycling Impact on TSV CV

Thermo cycling:
-40°C (15 min)
+125°C (15 min)

No significant change in TSV C-V behavior before and after thermo-cycling.
CV-t: Detect Barrier Integrity Issues

On the Determination of Minority Carrier Lifetime from the Transient Response of an MOS Capacitor

FREDERIC P. HEIMAN, MEMBER, IEEE

Fig. 1. Relaxation of depletion region due to generation of electron pairs in the depletion region of an MOS capacitor for negative voltage.

Fig. 2. Normalized C-V curve for bulk silicon MOS capacitor. Fast sweep shows deep depletion. Experimental transient response for capacitor whose C-V curve is shown in Fig. 2. Slope yields lifetime of 7.6 μs.

- Lifetime of carriers is extracted from slope
- Change of lifetime is indicating Cu migration into Si
Thermo-Cycling Impact on C-t

- Barrier Integrity preserved after thermo cycling
- Charges in oxide useful for capacitance reduction are harmless and do not deteriorate C-V and C-t behavior after thermo-cycling

No significant change in TSV C-t behavior before and after thermo-cycling
3D-Reliability Domains

- TSV
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Control of Copper Pumping

Does the pumping damage interconnects above it?
TSV impact on M1

M1 meanders around TSVs

M1 Meanders with and without TSVs

No evident impact of TSV
M2 meander-fork structures running above TSVs

TSV impact on M2

No evident impact of TSV
**TSV Stress Impact on Transistors**

- Good agreement of model and Si data
- No fitting necessary, just using measured Cu properties
Temperature Impact on TSV Stress

- Stress drops with temperature: Cu/Si thermal mismatch
- Linear trend suggests elastic stress behavior
- Will storage/operation temperature affect this?
Temperature Impact on TSV Stress

– Test approach
  • $I_{on}$ before and after thermal storage and cycling

– Test material
  • HKMG gate stack CMOS technology
  • TSV’s: 5$\mu$m wide, 40$\mu$m deep
  • Two splits in plating chemistry (Chem. D and Chem. E)

– Test structure
  • Long channel pMOS devices (from DAC Array)
  • Reference transistors: > 20$\mu$m away from TSV
  • Transistors close to TSV: 1.7$\mu$m away from TSV
  • Today: Focus on transistors below TSV (i.e. transverse)
Temperature Impact on TSV Stress

Results before aging

Proposed aging tests

- 1 week at 175°C (↑ eZST for chem. D and ↓ eZST for chem. E)
- 150 cycles between -45°C and 125°C
Temperature Impact on TSV Stress

Results after aging

Proposed parameter: Ratio between %-difference before and after thermal stress

- T-storage below eZST (chem. D) ➔ Stress increases
- T-storage above eZST (chem. E) ➔ Stress reduces
- T-cycling has even bigger impact
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3D Stacking Approaches


- Process of Record: Cu/Sn
- Scaling: 40→20µm

Cu/Sn Transient-Liquid-Phase, TLP, (250°C)

Diffusion bonding (150°C)
Micro-Bump Impact on N-FET Array

• Objective
  – Determine Impact of ubump on long channel N-type logic devices

• Method
  – Compare Ion of Ref FET array with ubump FET array on stacked dies w/wo NUF
  – Device size = 800 x 600nm
  – 16x16 FET array
Micro-Bump Impact on N-FETs

REF FET w/o Ubump

FET with Ubump

Normalized $I_{ON}$ vs REF

Huge, 40% NMOS current impact!
Under-Fill Impact on N-FETs

ETNA stacks with NUF

Cross-section for comparison

ETNA stacks w/o NUF

No underfill – no stress
• Combination of ubump and NUF has been identified as the main contributor of stress on thinned dies (25µm)

• Stress induced by ubump w/o NEF on the FEOL is around 5%

This effect is easy to model

There is apparent ubump misalignment
Ubump Stress at Elevated T

Cross-section on FET row 6

Stress drops with temperature

Normalized Ion change wrt reference MOS position in row 6 of FET array

FET Column 1
FET Column 16

Ubump

Ubump Stress at Elevated T

Stress drops with temperature

Normalized Ion change wrt reference MOS position in row 6 of FET array

Ubump

Ubump Stress at Elevated T

Stress drops with temperature

Normalized Ion change wrt reference MOS position in row 6 of FET array

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Ubump

Ubump Stress at Elevated T

Stress drops with temperature

Normalized Ion change wrt reference MOS position in row 6 of FET array

Ubump
Ubump Stress vs Temperature

- Stress drops with temperature: Cu/NUF thermal mismatch
- Linear trend suggests elastic stress behavior

Close to linear change of Ion versus T from 25°C to 80°C

Equivalent Zero Stress Temperature (eZST) is around 160°Celsius

Linear extrapolation shows 55% change at 0 degrees
Modeling Micro-Bump Stress

- Hill top (biaxial tensile)
- Valley bottom (biaxial compr.)
- Saddle point (tensile $S_{xx}$ but compr. $S_{yy}$)
- Saddle point (compr. $S_{xx}$ but zero $S_{yy}$)

Shrinking NUF bends the thin die around the strong $\mu$-bump
Modeling Micro-Bump Stress

Map of vertical displacement (vertical scale exaggerated)

Non-circular features due to anisotropic Si crystal properties

Hills over \( \mu \)-bumps, valleys in between
Electron Mobility Map: 48% Range

Strong hills, weak saddles, neutral valleys
Hole Mobility Map: 77% Range!

Strong longitudinal saddles, weak transverse saddles, but neutral hills and valleys
Summary

- Experimental and theoretical investigation of several key 3D IC reliability issues
- Strong TSV stress effects: 5% Ion for analog PFETs and 20% for digital FETs
- Even stronger micro-bump stress effects on NMOS: > 40%
- TSV pumping effect is analyzed and mitigated
- CV and C-t measurements confirm no Cu gets into oxide/Si
- Significant drift of TSV stress is discovered both for thermal storage and for thermal cycling: up to 35% current shift
- Proposed measurement techniques can be used to characterize different aspects of 3D IC reliability
- Proposed modeling methodology can be used to analyze and ensure reliable TSV implementation