Metal Gate / High-k Reliability Characterization:
From Research to Development and Manufacturing

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Motivation

- Metal gate / high-k MOS process and device research has emerged in the past decade and is used in CMOS technologies since the 45nm technology node.

- To further increase the confidence in the use of MG / HK it is important to address reliability issues both from scientific and engineering perspectives.

  - Generate fundamental understanding about defect generation and its implication on reliability projection (BTI, TDDB, hot carrier degradation, ...)

  - Introduce novel characterization procedures that properly capture the degradation processes.
Outline

- Introduction
- Metal Gate / High-k (MG/HK) background
- Bias temperature instability (NBTI, PBTI)
- Stress-induced leakage current (SILC) in nFET devices
- Dielectric breakdown
- Summary
- Outlook
Introduction

The use of MG HK presents the biggest change in gate stack in the last decade and thus requires thorough reliability investigations.
Introduction (cont)

- Substantial learning in electrical characterization and
  reliability has been made for MG HK devices
  throughout the years:
  - Negative bias temperature instability (NBTI) remains a
    reliability challenge for pFET devices
  - Positive bias temperature instability (PBTI) emerged as
    reliability challenge for nFET devices
  - Stress-induced leakage current increase reported for nFET
    devices
  - Time dependent dielectric breakdown (TDDB) complicated by
    the dual-layer nature of the gate dielectric stacks
  - Further reliability topics remain important for MG HK CMOS
    technologies (e.g., hot carrier degradation, low frequency
    noise, ... )
MG HK background: Integration Approaches

- High-k-first / metal-gate-last process flow → “quasi replacement”
- Gate-first integration scheme with high-k/metal gate electrodes

TEM of Intel high-k + metal gate 45 nm PMOS transistor

TEM of IBM high-k + metal gate 45 nm NMOS transistor

K. Mistry et al., p.247, IEDM 2007

M. Chudzik et al., p.194, VLSI 2007
MG HK background: Gate Stack and nFET Band Diagram

- Basic gate stack structure contains interlayer, high-k dielectric, and metal electrode
- To meet band-edge work function either metal electrode tuning, capping layers, or substrate engineering are typically employed
MG HK background:
Gate Tunneling Currents / Carrier Separation

- For nFETs, inversion layer electrons are the dominant contributor to the tunneling current at operation and stress condition
- For pFETs, hole and electron tunneling become comparable at stress condition
MG HK background:
NBTI / PBTI comparison MG HK versus Poly-Si / SiON

- NBTI for MG HK comparable to conventional poly-Si / SiON stacks
- PBTI emerged as reliability challenge for MG HK nFET devices
Similar time evolution for MG / HK NBTI and PBTI
Power law time exponents ranging between 0.18 and 0.13, which are comparable to conventional poly-Si / SiON stacks
Note the gradual change in slope → saturation behavior
PBTI Time Evolution versus Sense Delay

- Significant impact of sense delay on PBTI shift and time evolution → fast measurement techniques essential to capture worst-case shift and to improve projection model
To first order, the $\Delta V_t$ recovery can be modeled by a log(t) dependence

Linear relation between $\Delta V_t(1s)$ and $\alpha$ for short stress and low shifts
Log(t) recovery corresponds to 1/t recovery rate \( \Rightarrow \) charge removal by tunneling the likely cause

- Striking similarities between conventional poly-Si / SiON and MG HK stacks
Impact of Stress Mode on PBTI Relaxation

- Relaxation after AC stress shows shallower slope at short times and merges with DC relaxation at longer times.
- Relaxation modulated by stress time and duty cycle.

**Graphs:**
- **Relaxation time (sec)** vs. ΔVtlin (a.u.)
  - DC stress
  - AC 50% duty cycle
  - T = 50 °C
  - Vstress = 1.5 V

- **Relaxation Time (sec)** vs. ΔVtlin (a.u.)
  - DC
  - AC 99%
  - AC 90%
  - AC 50%
  - AC 10%
  - AC 1%
  - T = 50 °C
  - Vstress = 1.5 V

Impact of Stress Mode on PBTI Relaxation

K. Zhao et al., IRPS, pp. 50-54, 2009.

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Impact of Stress Mode on PBTI degradation

- Unipolar PBTI stress leads only to a shift in transistor characteristics ➔ bulk trapping
- Bipolar PBTI stress leads to shift and degradation of transistor characteristics ➔ bulk trapping and interface degradation
- Bulk trapping shows transient nature whereas interface degradation is permanent

SILC Polarity Dependence (poly-Si / HfO$_2$ nFET devices)

- Strong polarity dependence in SILC formation
  → for substrate injection one-to-one correlation between HfO$_2$ trap density and SILC
  → SILC traps believed to be different from pre-existing defects responsible for hysteresis

\[ \Delta J_{\text{stress}} = B \times t^n \]
\[ n = 0.65 \]
\[ B \propto e^{V_g} \]
nFET SILC Formation and Reversibility (TiN / HfO₂ nFET devices)

- Dramatic SILC reductions after negative bias discharge
- SILC ($\Delta I_g / I_g$) shows single broad peak and is attributed to electron traps in HfO₂

E. Cartier et al., IRPS, pg. 486, 2009.
nFET SILC Formation and Reversibility: (TiN / HfO$_2$ nFET devices)

- Oxygen vacancies charged during positive gate stress resulting in TAT sites

E. Cartier et al., IRPS, pg. 486, 2009.
A. Kerber et al., IRPS, pg. 505, 2009.
Double peak observed in SILC when stress at high temperature
- Deeper energy level, P1, defect either generated in the interlayer or in the HfSiOx
- Shallower energy level, P2, only generated during high-temperature stress and attributed to a defect in the HfSiOx layer
Alternative Interpretation of SILC ("SEMATECH view")

- Strong correlation between charge pumping and SILC
  → If CP only probes the interlayer, SILC is caused by interlayer defects !?!

G. Bersuker et al., IEDM, pg. 791, 2008

SILC Improvement by Process Optimization

- SILC improvements feasible by process optimization
  → Layer thickness engineering or change in materials property??
- Strong correlation between t63% and gate leakage current for both nFET and pFET devices
MG HK TDDB failure distributions

- Change in Weibull slope clearly evident for nFETs
- For pFET devices, change in slope only obvious when distribution is extended using larger areas
- Poisson scaling / vertical area scaling remains valid
Implication of Gradual Change in Failure Distribution

- Area-to-time transformation fails because the underlying distribution is not standard Weibull

\[ F(t) = 1 - \exp\left(-\left(\frac{t}{t_{63\%}}\right)^\beta\right) \]

A. Kerber et al., IRPS, pg. 505, 2009.
Explanation for Change in Failure Distribution with Gate Area

- **Competing degradation of a dual layer gate stack**
  - Failure distribution well described by applying the percolation concept with the assumption of different defect generation rates for interface and high-k layer

- **Progressive failure**
  - Because failure distributions are comparable to ultra-thin SiON/poly-Si stacks; it is also feasible that a similar concept may also apply to MG HK
  - Current time traces, however, do not support a very significant contribution to the change in failure distribution

- ...
BTI Screening and Monitoring of MG HK (Voltage ramp stress)

- Voltage shift based on VRS and CVS are well correlated
  \[ \Delta V_T(t, V_g) = A t^n V_g^m \]
  preferred screening procedure because limited knowledge about the gate stack is required


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TDDB Screening and Monitoring of MG HK (Voltage Ramp Stress)


- Good quantitative agreement between CVS and VRS breakdown data
Summary

- Compared to conventional CMOS technologies, PBTI and SILC in nFET devices are confirmed as emerging technology challenges for MG HK
  - PBTI shows similar magnitude and kinetics as NBTI and also comparable recovery behavior
  - SILC remains controversial because it is attributed to trap-assisted tunneling through either HfO$_2$ defects or inter-layer defects
- MG HK TDDB shows strong correlation with gate leakage current and thus serves as figure of merit for process development
  - Change in failure distribution is observed towards large areas / low failure percentiles ➔ dual layer percolation model was introduced for MG HK
- For monitoring and process screening, Voltage ramp stress is proposed, which is in good quantitative agreement with the CVS method
Outlook

- Attempts have been made to demonstrate defect generation and identify the defect nature in MG HK stacks, but the literature still remains controversial.

- Some of the open questions are:
  - Trap filling versus trap generation during PBTI??
  - Why are NBTI and PBTI kinetics, including recovery, so similar??
    - Can MG HK provide a better inside-into reaction-diffusion versus hole trapping??
  - What are the controlling parameters for SILC??
    - Material property or just thickness engineering
    - Is it of concern for higher temperature applications??
      (e.g., automotive & industrial)
  - Where does defect generation occur??
    - Interlayer, high-k layer, or both??
  - What is the correlation between SILC defects and TDDB??
  - ....