Charge-trap memories and 3D approaches

G. Molas et al.
Outline

- Limitations of Flash memories
- Engineering of the gate stack of planar TANOS-like memories
- 3D Charge trap memories
- Modelling and simulations
- Conclusions
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Introduction

Context
Difficulty of scaling standard existing FG Flash memories below the 30nm

- Physical scaling: cross coupling, FG sidewall suppression
  \[ \text{lower } \alpha_G \]

- Electrical scaling: SCE, low \( I_{\text{on}} \) due to W reduction

- Reliability scaling: SILC, ↓ of number of electrons
  (G. Molas et al., IEDM 2004, TED 2006)...

\[ \text{New solutions under investigations: high densities, low disturb and cross coupling, good memory cell scalability (low SCE...), good reliability...} \]
Context – Flash scaling

<table>
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<tbody>
<tr>
<td>NAND Flash Technology [nm]</td>
<td>51</td>
<td>45</td>
<td>40</td>
<td>36</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
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<tr>
<td>Cell type</td>
<td>FG</td>
<td>FG</td>
<td>FG</td>
<td>FG/CT</td>
<td>CT</td>
<td>CT</td>
<td>CT-3D</td>
<td>CT-3D</td>
<td>CT-3D</td>
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<tr>
<td>Floating gate</td>
<td>ONO</td>
<td>ONO</td>
<td>ONO</td>
<td>ONO</td>
<td>ONO</td>
<td>High-k</td>
<td>High-k</td>
<td>High-k</td>
<td>High-k</td>
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<tr>
<td>NAND Interpoly</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Interpoly thickness [nm]</td>
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<td>10-13</td>
<td>10-13</td>
<td>10-13</td>
<td>10-13</td>
<td>9-10</td>
<td>9-10</td>
<td>9-10</td>
<td>9-10</td>
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</tbody>
</table>

ITRS envisages High-k interpoly combined with charge trapping (CT) layers for sub-30/20nm nodes to maintain high coupling ratio and good reliability. 3D forecasted to replace planar to increase the density

→ TANOS and SONOS envisaged in planar and 3D architectures for future memory generations

Planar TANOS 63nm SAMSUNG IEDM’05

3D Charge trap memories (Toshiba, Samsung…)
Our Approach

TANOS memories suffer from integration issues:

- Retention degradation at high temperature (low Si$_3$N$_4$/Al$_2$O$_3$ energy barrier)
- High program erase voltages
- Compromise between retention and erase difficult to achieve

In this context:

- We propose the engineering of the TANOS gate stack to improve the memory performances
- 3D solutions are proposed for future generations
- Physical mechanisms governing the TANOS memory are analyzed based on models and simulations
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Improving the retention of TANOS memories

$\text{SiO}_2 / \text{Al}_2\text{O}_3$ as topox
- Band engineered effect
- Same EOT (thinner $\text{Al}_2\text{O}_3$)

Lifetime ($\Delta V_T/\Delta V_{T0}=90\%$) [s]

$1/kT$ [eV]

Charge trap memories & 3D – ISAGST 2010
TANOS improvement - Tunox engineering

**Improving the PE speed of TANOS memories**

*HfSiON as tunox*
- Band engineered effect
- Low trap density

Band Engineered tunox: Higher PE speed compared to SANOS/TANOS references

Charge trap memories & 3D – ISAGST 2010
TANOS with HfSiON as tunox – Retention

125°C retention

1.5V of charge loss after 10 years

Same activation energy (0.3eV) than TANOS

Arrhenius graphs

Fast initial charge decay

1.5V of charge loss after 10 years

Same activation energy (0.3eV) than TANOS
Improving retention of TANOS memories

**AlN as CTL**
- Deep traps
- Large bandgap
- High trap density

Better PE speed and better retention expected

16V 100µs
-16V 10ms

6.5V
3V
-16V

Charge trap memories & 3D – ISAGST 2010

G. Molas
September 30th 2010
TANOS with AlN/Si$_3$N$_4$ charge trapping layer

Electrons trapped in the Si$_3$N$_4$ layer see a « thick » WKB barrier due to the AlN bottom layer

→ Reduced leakage current and improved retention

→ AlN-based CTL: High PE speed, good cycling and retention
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Monolithic 3D Memory Architectures

P-BiCS

**Toshiba** Katsumata, VLSI 2009

TCAT

**Samsung** Jang, VLSI 2009

VSAT

**Samsung** J. Kim, VLSI 2009

VG-NAND

**Samsung** W. Kim, VLSI 2009

VG-TFT-NAND

**Macronix** H. Lue, VLSI 2010

Strong interest on 3D approaches, various architectures are investigated.
3D nanowire SONOS memories – Process flow

1. Selective epitaxy of (Si/SiGe)
2. Si anisotropic dry etching
   + SiGe dry isotropic etching
   2.1 Dry sacrificial oxidation
   + H2 annealing
3. ONO deposition
   O/N/O = 6/5/8nm
4. Poly-Si N+ deposition
   + Chemical Mechanical Polishing
   + Gate etching
   + S/D implantation
   + Nitride spacers
   + S/D salicidation
   + BEOL

A. Hubert et al., IEDM 2009

Charge trap memories & 3D – ISAGST 2010

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Gate-All-Around (GAA) SONOS memory with «crystalline» Si nanowire channels (down to 6nm diameter)

A. Hubert et al., IEDM 2009
3D nanowire SONOS memories – results (1/2)

Program Erase

Acceptable erased saturation phenomenon is observed for a N+ Poly-Si gate

A. Hubert et al., IEDM 2009

Cycling

ΔV_{Th} is only shifted by 0.8V after 10K cycles
3D nanowire SONOS memories – results (2/2)

Retention

At 25°C retention shows 18% charge loss ($\Delta V_T \sim 4.6\text{V} \text{ after 10ys}$)
Even at 200°C, 50% of the charge is maintained

A. Hubert et al., IEDM 2009

Geometry

GAA SONOS Nanowire with small cylinder shape greatly enhances the programming efficiency

10 12 14 16 18 20

10 2 4 6

0 25 50 75 100%

Normalized $V_{Th}$ Shift

Retention Time (s) 10 years

0% 25% 50% 75% 100%

$\Delta V_{Th}$

Stress Voltage $V_G$ (V)

10 12 14 16 18 20

O/N/O: 6/5/8nm

$W_{Si} \sim 6\text{nm}$

$W_{Si} \sim 16\text{nm}$

$W_{Si} \sim 26\text{nm}$

FinFlash

$\sim 25\text{°C}$

$\sim 125\text{°C}$

$\sim 200\text{°C}$

82%

72%

50%

82%
New 3D memory architecture with crystalline channels

Technology can be derived from the stacked GAA SONOS Silicon nanowire developed process
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  - Trapping properties of Si$_3$N$_4$ layers
  - Leakage through Al$_2$O$_3$ control dielectrics
- Conclusions
Understanding the electrical behavior of SiN memories

Experimental study

Results show same program, different erase and retention

→ Intrinsic difference in the trapping properties of std and Si-rich SiN

E. Vianello et al., IEDM 2009, IMW 2010

In collaboration with Univ. of Udine
Defects types from material studies: $\beta$-Si$_3$N$_4$ with H (SIMS + MIR)

<table>
<thead>
<tr>
<th>Defects</th>
<th>Trap density</th>
<th>$Q_N$</th>
<th>$n^T$</th>
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<tbody>
<tr>
<td>Std SiN</td>
<td>Si-H</td>
<td>$N_T^{\text{Si-H}}$</td>
<td>-$q.n^T$</td>
</tr>
<tr>
<td>Si-rich SiN</td>
<td>Si-H, Si dB</td>
<td>$N_T^{\text{Si-dB}} + N_T^{\text{Si-H}}$</td>
<td>-$q.(n^T-N_T^{\text{Si-dB}})$</td>
</tr>
</tbody>
</table>

Atomistic simulations of defects on SiN layers

Extraction of the defects parameters from atomistic simulation

$\Delta Q_N = 1e^-$, causes the $\Delta V_T$

$Q_N(x,t)$ is the excess charge w.r.t. neutral SiN → $Q_N$ causes the $V_T = f(Q_N)$

$n^T(x,t)$ is the electron concentration in the higher energy states → $n^T$ influences the charge loss $J = f(n^T)$
Device 1D physical modelling

(1) Tunnel-In (FN, DT, mFN, B-T)

(2) Electron transport + capture/emission
   - Motion of electrons in SiN: Drift-Diffusion
   - Interaction between the electrons in the CB and in the energy gap
   - **Emission rate** (Poole-Frenkel)

(3) Tunnel-Out
Simulation of the electrical behaviour of SiN memories

Modeling of the Program Characteristics

*Parameters of defects from atomistic simulations*

- Programming is driven by the $e^-$ injection from substrate ($Q_N$)
- Similar program transients in std and Si-rich SiN

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E. Vianello et al.,
IEDM 2009
Simulation of the electrical behaviour of SiN memories

Modeling of the Retention Characteristics

Parameters of defects from atomistic simulations

Same EOT and initial $V_T$ $\rightarrow$ same electric field in the stack

double occupation number $(n^T)$ $\rightarrow$ larger charge loss in Si-rich SiN
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H-related defects in Al$_2$O$_3$ – from atomistic to device simulation

Atomistic calculations  ➔  Device simulations  ➔  Experimental results

O vacancies and H-related defects in Al$_2$O$_3$ play a major role in the trapping properties

Implementation of H-defects in the Al$_2$O$_3$ TAT conduction of TANOS memories (1D simulator)

H-related defects can degrade retention of TANOS memories ➔ High T°PDAs reduce H content and improve retention

→ To be presented at IEDM 2010
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Conclusions

Optimization of the TANOS gate stack
- TANOS memories: reliability issues (poor retention)
- Engineering of the gate stack (tunnel oxide, charge trapping layer, control dielectrics) allows to improve the memory performances

Monolithic 3D
- Crystalline Si-channel (no grain boundaries)
- Integration of various memory morphologies
- Double gate operation possible with Φ-Flash memories
- GAA: excellent gate coupling (Φ_Si down to 6nm)
- Good memory performances (fast PE, low T° activation)
- Towards a full 3D memory with crystalline Si channels

Modelling and simulations
- Use of device simulations based on atomistic calculations
  - Defects of different nature (linked to H and excess Si) dominate the trapping properties of stoichiometric and Si-rich SiN
  - Strong role of O-vacancies and H-related defects in Al_2O_3 on TANOS retention
Acknowledgments


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+ Univ. of Modena, Italy
References

Innovation for industry