A Survey of Cross Point Phase Change Memory Technologies

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Sematech International Symposium on Advanced Gate Stack Technology

Sep/30/2010
Hilton Garden Inn, Troy, NY
Outline

• Overview and Motive
  – Storage Elements
  – Selector Elements
  – Why thin film based Cross Point Array
• Cross Point Phase Change Memory Array
  – Thin film two-terminal switches
  – Array operations
• PCMS in Computing Memory Hierarchy
  – PCMS characteristics
  – Performance benchmark
• Summary
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Simple resistor 1-D steady state approximation:

Fourier’s Law

Ohm’s Law

Continuity Equation

\[
\frac{d^2T(x)}{dx^2} = -\frac{J^2 \rho}{\kappa}
\]

\[
I_{\text{write}} = \frac{A}{L} \sqrt{8 \frac{\kappa}{\rho} \left(T_{\text{peak}} - T_0\right)}
\]

\[
V_{\text{write}} = \sqrt{8 \kappa \rho \left(T_{\text{peak}} - T_0\right)}
\]
Critical Area = $[\alpha \cdot \lambda]^2$

$I_{reset} = 2 \cdot (\alpha \cdot \lambda)^{1.5}$
Phase Change Material Engineering

SET Energy-Bandwidth

![Graph showing voltage, pulse length, and resistance](image1)

Nanosecond switching in GeTe

Retention and Disturb

![Graph showing data lifetime vs. inverse temperature](image2)

T. Morikawa, *et al.*, iedm 2007,
Good Data Retention in In-Ge-Te
Heater, Electrode and Interface

Heater vs. Self-heat

Thermal Boundary Resistance and Electrical Interface Barrier

Reset temperature along center axis with (solid line) and without (dotted line) interfaces

David Kencke, *et.al.*, IEDM 2007, The Role of Interfaces in PCM
Vertically Integrated PCM

Y. N. Hwang, et. al., VLSI ’03, T12B3

F. Pellizzer, et. al., VLSI ’06, T15P3

J. H. Oh, et. al., IEDM ’06, S2P6

Y. Chen, et. al., IEDM ’03, S37P4

Y. Sasago, et. al., VLSI ’09, T2B-1

D. Kau, et. al., IEDM ’09, S27.1

DerChang Kau, ISAGST 2010, Troy, NY
Why thin film Cross Point PCM Architecture

• True Cross Point Array
  – Cell dimension: $4 \lambda^2$
  – Strapless to simplify routing and process

• Stackable
  – Low temperature process
  – CMOS under the memory
  – Compatible with mainstream backend process
  – Multiple decks feasible
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"A Survey of Semiconductor Devices"

Diode: two terminals and exhibiting a nonlinear I-V (*IEEE Standard Dictionary*)

- **Rectifiers**
  - $V_{BD}$ vs. $I$
  - $V_f$ vs. $I$

- **N-Shape**
  - $I$ vs. $V$
  - $V$ vs. $I$

- **S-Shape**
  - $I$ vs. $V$
  - $I$ vs. $t$

- **Transient**
  - $I$ vs. $t$
  - $V$ vs. $t$

---

Fig. 4. Different devices that can be called switches. Examples are: (a) rectifier, (b) transistor, (c) thyristor, and (d) two-terminal switch.

Kowk Ng, IEEE EDS Distinguished Lecture SCV Chapter, 11/7/05
Thin Film Diode Candidates for Cross Point PCM

Y. Sasago, et. al., *VLSI ’09. T2B-1*

M. Lee, et. al., *IEDM ’07, S30.2*

W Y Park, et. al., *Nanotechnology 21 (2010) 195201*

K. Gopalakrishnan, et. al., *VLSI ’10. TS19.41*

D. Kau, et. al., *IEDM ’09. S27.1*
### I-V Phenomenology

<table>
<thead>
<tr>
<th>Poly Junction</th>
<th>Oxide Junction</th>
<th>Oxide Rectifier</th>
<th>MIEC</th>
<th>OTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si PN junction</td>
<td>Ox PN junction</td>
<td>Pt/TiO₂/Ti</td>
<td>Cu⁺ in SE</td>
<td>Chalcogenide</td>
</tr>
<tr>
<td>Minority carrier;</td>
<td>Minority carrier;</td>
<td>Schottky barrier</td>
<td>Schottky barrier modulated</td>
<td>Ovonic Threshold</td>
</tr>
<tr>
<td>drift + diffusion</td>
<td>drift + diffusion</td>
<td>+ Filamentary</td>
<td>by Ionic motion.</td>
<td>Switching</td>
</tr>
<tr>
<td>Sub nsec</td>
<td>10 to 100 nsec*</td>
<td>Forming/dissolving</td>
<td>~100ns forming</td>
<td>nsec switching &amp; recovery</td>
</tr>
<tr>
<td>Unidirectional</td>
<td>Unidirectional</td>
<td>Unidirectional</td>
<td>Bidirectional</td>
<td>Bidirectional</td>
</tr>
<tr>
<td>&lt; 10MA/cm²</td>
<td>&lt; 0.1MA/cm²</td>
<td>&lt; 1MA/cm²</td>
<td>50MA/cm²</td>
<td>Match PCM</td>
</tr>
</tbody>
</table>

![Graphs and Images](image)

- Y. Sasago, et al., VLSI ’09. T2B-1
- M. Lee, et al., IEDM ’07, S30.2
- W. Park, et al., Nanotechnology ’10
- K. Gopalakrishnan, et al., VLSI ’10. TS19.41
- D. Kau, et al., IEDM ’09. S27.1

*: Huang et al., Sci. in China, Physics, Mechanics & Astronomy 2005 Vol.48 No.3 pp.381--384
Advances in Thin Film Switches Beyond “Traditional Rectifier”

• **Competency** – Semiconductor fabrication maturity improves device reproducibility and cumulative learning

• **Challenge** – The switching transient such as filamentation requires proper DUT design using non-equilibrium characterization technique.

• **Novelty** – The physics of resistive switching mechanisms fuel innovations on the new classes of selectors
Cross Point Array Operations: Access

**Unidirectional Rectifier**

A rectifying selector turns on one bit with forward bias and isolates others with reverse bias.

**Bidirectional Switch**

Subject to the potential drop at each cross points, the selected bit is triggered and the unselected bits are blocked.
Reading a PCM in Cross Point Array

- To interrogate PCM state, PN diode or MIEC is turned ON to sense the current.
- With a S-Shape Selector like OTS, threshold demarcation is used for Read.
- MLC is perceived easier with a non-NDR selector; however, variability of bias points needs to be carefully controlled due to superlinear I-V characteristics.
- Demarcation Read with a S-Shape Cell is inherently faster due to NDR.

**PCM IV; 4 levels programmed**
Writing a PCM in Cross Point Array

• Sub-lithographic features have been deployed to reduce $I_{\text{RESET}}$
  – Manufacturing latitude of those innovations becomes increasingly restricted as technology scales.
  – $I_{\text{RESET}}$ is converging with various device structures

• Areas of focus:
  – Electrical interface and thermal boundary properties such as cell confinement and architecture
  – SET Kinetics in Nano-geometry for energy efficiency
  – PCM’s high speed vitrification capability must not be hindered by the thin-film selector in series.
  – Selector and electrodes becomes the liability to endurance as RESET current density increases.
Array Parasitics

- The parasitic R and C consume operating energy.
- Displacement current during access is dissipated mostly on the intra layer capacitance and decoding circuit.
- Array consumes leakage power when unselected cells are biased.

**Example: Single deck Cross Point PCM array with “C” bit-lines and “R” word-lines**

<table>
<thead>
<tr>
<th></th>
<th><strong>Unidirectional Rectifier</strong></th>
<th><strong>Bidirectional Switch</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sel. WL</td>
<td>C-1</td>
<td>C-1</td>
</tr>
<tr>
<td>Sel. BL</td>
<td>R-1</td>
<td>R-1</td>
</tr>
<tr>
<td>DeSel Cells</td>
<td>(C-1)•(R-1)</td>
<td>(C-1)•(R-1)</td>
</tr>
<tr>
<td># of Cell</td>
<td>C-1</td>
<td>C-1</td>
</tr>
<tr>
<td>Switching</td>
<td>0</td>
<td>1 row</td>
</tr>
<tr>
<td></td>
<td>1 col</td>
<td>1 col</td>
</tr>
<tr>
<td></td>
<td>(R-1) rows</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>(C-1)•(R-1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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State of the Art Computing Memory Hierarchy

• Imperatives on cost vs. performance in memory subsystem
  – performance increases as it moves closer to processors
  – Capacity of each subsequent level increases by roughly one order

• Challenges to a disruptive innovation between NAND & DRAM
  – DRAM latency will be sustained and throughput will improve.
  – NAND will maintain or improve performance with cost leadership

<table>
<thead>
<tr>
<th>Memory Subsystem</th>
<th>Normalized Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Cost</td>
</tr>
<tr>
<td>On-chip SRAM</td>
<td>&gt; 10</td>
</tr>
<tr>
<td>Component DRAM</td>
<td>1</td>
</tr>
<tr>
<td>SSD NAND</td>
<td>0.1</td>
</tr>
<tr>
<td>Form factor HDD</td>
<td>&lt; 0.01</td>
</tr>
</tbody>
</table>

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PCMS Array Construction

D. Kau, et.al.,
IEDM ’09, S27.1
PCM vs. PCMS

**Diagram:**
- **DOE Split:** with vs. without OTS
- **Graph:**
  - Y-axis: $\Delta Vt [\%]$
  - X-axis: Pulse Amplitude [%]
  - Two curves: PCM and PCMS
  - PCM curve starts lower and remains lower than PCMS throughout the graph.

**Text:**
- OTS improves PCM RESET effectiveness.
PCMS Cross Point Array RESET Speed

High speed RESET capability is validated with Cross Point Array
PCMS Array Cycling Endurance

Degradation tails (3.5σ) developed after 1 million S/R cycles.
Program Distribution

A good candidate for high density components
## Benchmark of Computing Memory

### 34nm NAND vs. DDR3 DRAM vs. projected 34nm PCMS

<table>
<thead>
<tr>
<th>Memory</th>
<th>NAND</th>
<th>PCMS</th>
<th>DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Normalized Cost</strong></td>
<td>0.1</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Normalized Bandwidth</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>READ</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>RESET</td>
<td>0.05</td>
<td>0.5</td>
<td>1</td>
</tr>
<tr>
<td>SET</td>
<td>&gt; 10</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td><strong>Normalized Latency</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>READ</td>
<td>1K</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>RESET</td>
<td>20K</td>
<td>3~5</td>
<td>1</td>
</tr>
<tr>
<td>SET</td>
<td>60K</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td><strong>Endurances (cycles)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10K</td>
<td>&gt; 1M</td>
<td>&gt;1E15</td>
</tr>
<tr>
<td><strong>Disturb (cycles)</strong></td>
<td>10K</td>
<td>&gt; 1E12</td>
<td>N/A</td>
</tr>
</tbody>
</table>

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Summary

• Thin film PCM Cross Point Arrays possess cost advantages
  – “Cross Point” means $4 \lambda^2 / \text{Cell}$ for each deck of memory
  – “Thin film” enables multi-deck to amortize cell size.
  – “Thin-film-Cross-Point” array is stackable over CMOS to reduce die size

• The Physics on resistive switching fuel innovations on thin-film diodes
  – OTS is a strong contender among all the thin film diodes;
  – It’s a bidirectional threshold switching element to isolate PCM cell;
  – it scales with PCM, physically, chemically & electrically

• Cross Point PCMS Array demonstrates
  – Near DRAM performance with good NVM reliability
  – Cost comparable to NAND

PCMS fits well between NAND & DRAM in computing memory hierarchy
Acknowledgement

• I would like to thank to Intel NVM team for helpful discussions

• I would also like to acknowledge the authors of the literature referred here