Recent Advancements in Spin-Torque Switching for High-Density MRAM

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Outline

• Current status of MRAM products
• Toggle MRAM and Spin-Torque MRAM in the memory landscape
• Recent advancements in Spin-Torque MRAM technology
• Summary and Future Prospects for MRAM
Everspin Introduction

- Formed as Everspin in June 2008 – Previously part of Freescale Semiconductor
- The leading developer and manufacturer of integrated magnetic products
  - Industry-first MRAM supplier since June 2006
  - Embedded MRAM systems
  - Integrated magnetic sensors
- Current MRAM products
  - Parallel interface products ranging from 256k-16Mb
    - Infinite endurance, >20 year data retention, 35 ns read & write speed
  - Serial interface products ranging from 256kb-1Mb
    - 40 MHz SPI interface, No write delay, infinite endurance
# Everspin MRAM Advantages

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Capability</th>
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<tbody>
<tr>
<td>Non-volatile capability</td>
<td>• Data retention &gt;20 years</td>
</tr>
<tr>
<td>Performance</td>
<td>• Symmetric read/write – 35ns</td>
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<tr>
<td>Endurance</td>
<td>• Unlimited cycling endurance</td>
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<tr>
<td>CMOS integration</td>
<td>• Easily integrates in manufacturing back-end</td>
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<td>• Compatible with embedded designs</td>
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<td></td>
<td>• No impact on CMOS device performance</td>
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<tr>
<td>Temperature range, reliability</td>
<td>• -40°C &lt; T &lt; 150°C operation demonstrated</td>
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<tr>
<td></td>
<td>• Intrinsic reliability &gt; 20 years lifetime at 125°C</td>
</tr>
<tr>
<td>Soft error immunity</td>
<td>• MRAM cell radiation tolerant</td>
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<tr>
<td></td>
<td>• Soft error rate from alpha radiation too low to measure (&lt;0.1 FIT/Mb)</td>
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<tr>
<td>Environmentally friendly</td>
<td>• No battery, RoHS compliant, low power</td>
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Everspin MRAM Technology

- Simple 1-transistor + 1-MTJ memory cell
- MTJ inserted between metal layers
- State of bit detected as change in resistance
- Unlimited endurance
- Leverage CMOS semiconductor ecosystem
MRAM Storage Concept

Free Layer
Tunnel Barrier
Fixed Layer

Parallel = Low Resistance
Anti-Parallel = High Resistance

4Mb Measured Resistance Distribution

σ ~ 0.8%
MR ~ 28% @ 300mV w/ xstr

NiFe/AlOx/NiFe
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Memory Endurance Comparison

Everspin MRAM is the only Working Memory in the market that is Nonvolatile.
Memory Capacity Comparison

Current Everspin MRAM products are utilized as a Nonvolatile Working Memory in the market with performance/density similar to volatile SRAM.
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MRAM bit switching

**Toggle-MRAM in production**

- **Write architecture:** cross-point
  - Magnetic field pulses switch free layer
- **Read architecture:** 1T-1MTJ

**ST-MRAM in development**

- **1T-1MTJ architecture**
  - read and write
- **Spin torque from polarized tunneling current switches free layer**

- **Digit line write current**
- **H-field**
- **Isolation transistor**

- **Free layer**
- **Fixed layer**
- **Tunnel barrier**

- **Bit line write current**
Toggle Write Operation

Advantages: Eliminates disturb - Large operating window
Toggle-Bit Selection

- No \( \frac{1}{2} \)-select bit disturb
- All bits along \( \frac{1}{2} \)-selected current lines have increased energy barrier during programming
- Single write line can not switch bits
Spin Torque MRAM

Use spin momentum from current to change direction of $S$, $m$.

$$\Delta S = Torque$$

$\frac{\Delta S}{\Delta t}$

Free layer

Tunnel Barrier

Fixed Layer

Resistance ($\Omega$)

Current (mA)

Rmax

MR

Rmin

20 nm
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Distribution Considerations

- Separation of $V_{\text{switch}}$ and $V_{\text{breakdown}}$
  - *Tunnel barrier reliability*

- Separation of $V_{\text{read}}$ and $V_{\text{switch}}$
  - *Avoid read-disturb errors*

- Separation of distributions important for working memory
  - MB memory $\Rightarrow$ 12$\sigma$ separation

\[
\text{Separation} = \frac{V_{\text{bd}} - V_{\text{sw}}}{\sigma_{\text{avg}}}
\]
Separation of switching and breakdown

- Large separation provides operating window
- From 16 kb arrays integrated with CMOS
  - Distributions: $\sigma \approx 4\%$
- Nonvolatile: $E_b/k_B T \approx 60$
- Continue increasing separation for reliability and manufacturing margin
  - Goal is unlimited endurance
Scaling ST-MRAM

• Today: Reduce $J_c$ for reliability and smaller transistors
• Continued scaling: maintain energy barrier and manage distributions

• ST-MRAM bits scale favorably to available current from transistor
• Scaling requires continued improvement in magnetic devices and materials

$I_c$ calculated for $J_c=2\text{MA/cm}^2$
Summary

• **MRAM is a highly reliable, high-performance, nonvolatile memory ICs, with unlimited endurance**
  – Has the unique characteristics of a working memory while providing non-volatility

• **Current MRAM product densities ranges from 256kb-16Mb**

• **Spin-Torque MRAM technology is advancing rapidly toward manufacturability**
  – Enables higher densities and lower power
  – Goal is to gain advantages of spin-torque writing while maintaining MRAM’s unique characteristics of nonvolatility and unlimited endurance