Basics of RRAM based on transition metal oxides

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Outline

1. Introduction and overview of RRAM technology

2. Fundamental resistance switching operation

3. Challenges

4. Summary
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RRAM: Resistance Random Access Memory

RRAM based on oxides:

Defects (oxygen vacancies) in oxide material play a key role for the resistance switching.

RRAM based on metallic bridge:

Connection and disconnection of metallic bridge in the insulating matrix governs the resistance switching.

IRS: initial resistance state
LRS: low resistance state
HRS: high resistance state
Flash memory is one of the current most major NVM and the memory density of Flash memory is expected to be continuously increased.

Higher performance NVM is essential for the next generation, ultra-high speed broadband era. RRAM is one of the best solutions

- Data non-volatility
- Low power operation
- High speed operation
- High cycle endurance
RRAM R&D in the world

Research Center Julich (Nature Mater.)
IBM, Zurich Research Laboratory (MRS, Adv. Mater)
IMEC (Collaboration with Samsung, Hynics, Micron Technology)
IBM, Zurich Research Laboratory (MRS, Adv. Mater)
CNR-INFM, Italy (IEDM, MRS)
MINATEC (MRS)

Europe

Seoul National Univ. (IEDM2006, APL, Nature Nanotechnology)
KIST(APL), GIST(APL)
ITRI (IEEE, IEDM2008, 2009)

Asia

Spansion LLC (IEDM2005 & 2006, APL)
University of Houston (PCMO, APL2000)
Unity Semiconductor, SEMATEC (IEDM2011)
Stanford University (IEEE, APL)

SHARP (IEDM2006, Patents, IMW)
AIST(MRS, APL, JJAP)
ULVAC (MRS, Patents)
Osaka Univ., Kanazawa Univ.
Univ. of Tokyo (APL)
Kyoto Univ. (APL)
Tottori Univ. (APL)
NEC (APL, IEDM2009)
Fujitsu (NVMD, IEDM2007)
Panasonic (APL, IEDM2007, 2008)
Toshiba (Nikkei Microdevice)

USA
Operating current and speed in RRAM

Operating current

10mA

1mA

100μA

10μA

< 25 μA

Operating speed

10ns

100ns

1μs

10μs

High speed operation

Low current operation

Y. Hosoi et al., SHARP & AIST, IEDM2006

I. G. Baek et al., Samsung, IEDM2004

Z. Wei et al., Panasonic, IEDM2008

K. Tsunoda et al., Fujitsu, IEDM2007


H. Y. Lee et al., ITRI, IEDM2008

Y. Tamai et al., SHARP & AIST SSDM2008
Comparison with MOSFET drive current

These NMOS drive current was calculated for the gate width of 100 nm.

Operating current of RRAM can be lower than the MOSFET drive current, indicating that RRAM is appropriate for the low operating power technology.
Estimation on required cycle endurance:

- Writing frequency: 1Hz (1 time / 1 sec)
- A period of use: 1 yrs

\[ = 3.1 \times 10^7 \text{ sec} \]

A practical CE for 1 memory element is in the order of \(10^7\) times.

CE in RRAM exceeds current Flash memories

CE for single bit Flash memory

CE for multi-bit Flash memory
Memory element size miniaturization

- Large devices for the basic researches
- Submicron-scale devices

- 50 nm x 50 nm Cross-point structure (HP, Samsung)
- 50 nm \( \phi \) Al/PCMO/Pt device (GIST, IEDM2009)
- 30 nm x 30 nm TiN/HfOx/TiOx/TiN device (ITRI, IEDM2009)
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Oxygen ion/vacancy movement in oxide material

**Electromigration of defects in TiO$_x$**


Dark blue region contains higher density of V$_O$

\[
\downarrow V = 35 \text{ V, in vacuum}
\]

V$_O$ electromigration is possible and it piles up around the negatively biased electrode.

This electromigration can be regarded as the oxidation/reduction reaction of oxides at the interface, or, doping of defects to the interface.
Pt(BE)/TiO$_x$/Pt(TE) Switchable diode

5μm x 5μm Pt/TiO$_x$/Pt junction

Positive voltage pulse to TE → Negative voltage pulse to TE

H. Shima et al., APL 94, 082905 (2009)

BE: bottom electrode, TE: top electrode
Categorization by resistance switching area

Breakdown → filamentary conduction path

Pt/TiOx/Pt, 20 x 20 μm²
- Breakdown of junction
- Hysteresis (Rectification switching)

Rectification switching → conduction by whole area of the junction

No device size dependence

A clear device size dependence

Log_{10}(I_{+1.0V}(A))

Log_{10}(I_{-1.0V}(A))

(a) After breakdown (+0.1V)

Initial

Δ = 0.1

Pt/TiOx/Pt

(w=500ms)

-7.0V

(b) After breakdown (-0.1V)

Initial

Δ = 0.8

Log_{10}(A_{PIT}(μm²))

-12

-10

-8

-6

-4

-2

0

2.0

2.5

3.0

3.5

4.0
Categorization by operational voltage polarity

Forming → The first resistance switching

Reset → Switching from LRS to HRS
Set → Switching from HRS to LRS

- Unipolar resistance switching
  → Voltage polarities for set and reset are identical

- Bipolar resistance switching
  → Voltage polarities for set and reset are opposite
Electrode material dependent switching

- The stable operation mode depends on the TE material. For the precious metal (i.e. inert material), URS can be observed. On the other hands, BRS is preferred for the reactive electrode materials such as Ti.
# Electrode material dependent switching

Electrode material dependent operation in HfO$_x$-RRAM

- **Inert material:**
  - Pt, Au → URS

- **Reactive material:**
  - Ti, Ta, TiN → BRS

<table>
<thead>
<tr>
<th>BE</th>
<th>TE</th>
<th>HfOx thickness (nm)</th>
<th>Deposition method</th>
<th>Demonstrated switching operation</th>
<th>References</th>
</tr>
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<tbody>
<tr>
<td>Mo</td>
<td>Mo</td>
<td>20</td>
<td>ALD</td>
<td>URS</td>
<td>1</td>
</tr>
<tr>
<td>TiN</td>
<td>Pt</td>
<td>20</td>
<td>ALD</td>
<td>URS</td>
<td>2</td>
</tr>
<tr>
<td>Pt</td>
<td>Au</td>
<td>22</td>
<td>PLD</td>
<td>BRS</td>
<td>3</td>
</tr>
<tr>
<td>TiN</td>
<td>Ti</td>
<td>3 ~ 10</td>
<td>ALD</td>
<td>BRS</td>
<td>4</td>
</tr>
<tr>
<td>Pt</td>
<td>Pt</td>
<td>10, 20, and 30</td>
<td>RF magnetron sputtering</td>
<td>URS</td>
<td>5</td>
</tr>
<tr>
<td>Pt</td>
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<td>12</td>
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<td>6</td>
</tr>
<tr>
<td>TiN</td>
<td>Ru</td>
<td>20</td>
<td>ALD</td>
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<td>7</td>
</tr>
<tr>
<td>TiN</td>
<td>Ti</td>
<td>5 and 10</td>
<td>ALD</td>
<td>BRS</td>
<td>8</td>
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<tr>
<td>TiN</td>
<td>Au</td>
<td>27</td>
<td>AVD</td>
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<td>9</td>
</tr>
<tr>
<td>TiN</td>
<td>Pt</td>
<td>5 and 15</td>
<td>ALD</td>
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</tr>
<tr>
<td>Pt</td>
<td>TiN</td>
<td>20</td>
<td>DC sputtering</td>
<td>BRS</td>
<td>11</td>
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<td>TiN</td>
<td>AlCu, Ti, and Ta</td>
<td>10 and 20</td>
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<td>Pt and TiN</td>
<td>Au</td>
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<td>13</td>
</tr>
<tr>
<td>Pt</td>
<td>TiN</td>
<td>~ 8</td>
<td>Oxidation of Hf</td>
<td>BRS</td>
<td>14</td>
</tr>
<tr>
<td>TiN</td>
<td>Pt</td>
<td>~ 5</td>
<td>RF magnetron sputtering</td>
<td>URS</td>
<td>Present work</td>
</tr>
<tr>
<td>TiN</td>
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<td>~ 5</td>
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<td>Present work</td>
</tr>
</tbody>
</table>

BE: bottom electrode
TE: top electrode

The drift of oxygen ions (or oxygen vacancies) is considered to play a key role. When the oxygen ions are supplied from the oxygen reserving layer, the device is switched into HRS. On the other hands, when the oxygen ions are absorbed by the oxygen reserving layer, the device is switched into LRS. Namely, the electrochemical reaction (oxidation and reduction) is the mechanism of the resistance switching.

H. Akinaga and H. Shima, proceedings of IEEE, in press.
In LRS, the current conduction is governed by the spatially confined area, the temperature rise by Joule heating is expected. Therefore, nanoscale thermal management will be required for the ultimate miniaturization of memory cells.
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Since the resistance switching speed is very fast, especially for the switching process into LRS, i.e., for the forming and set processes, the reliable current regulation is required. From this viewpoint, 1T1R configuration is appropriate. *H. Shima et al. Appl. Phys. Lett. 93, 113504 (2008).*
The reactive electrode material can effectively decrease the forming voltage $V_F$ of TiN/high-$k$ oxide/Ti/TiN RRAM after the appropriate annealing process. Depending on the annealing condition and layer structures in the RRAM element, the leak current becomes too large.
Nanoscale characterization of oxides

HADEF-STEM image of high-k/Ti interface

Electron energy loss spectroscopy (EELS) is a powerful tool to characterize oxides with a nanoscale resolution. However, especially for the high-k oxide, the characterization of metal edge EELS signal becomes difficult because of the severe signal intensity decay. Development of nanoscale metrology for RRAM is crucial in order to improve the operating reliability of RRAM in association with the material characteristics.
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- The excellent memory properties of RRAM, high speed and low power operation, good cycle endurance and compatibility with the CMOS device miniaturization has been evidenced and the potential of RRAM as the best candidate for the nonvolatile memory in the next generation is being steadily consolidated.

- The comprehensive development including the circuit design, nanoscale thermal management, as well as the nanoscale metrology suitable for RRAM are crucial for the further improvement of RRAM operational performance.