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Maskless Meeting: Evolution of the SRC/DARPA Maskless Patterning Initiative

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Overview

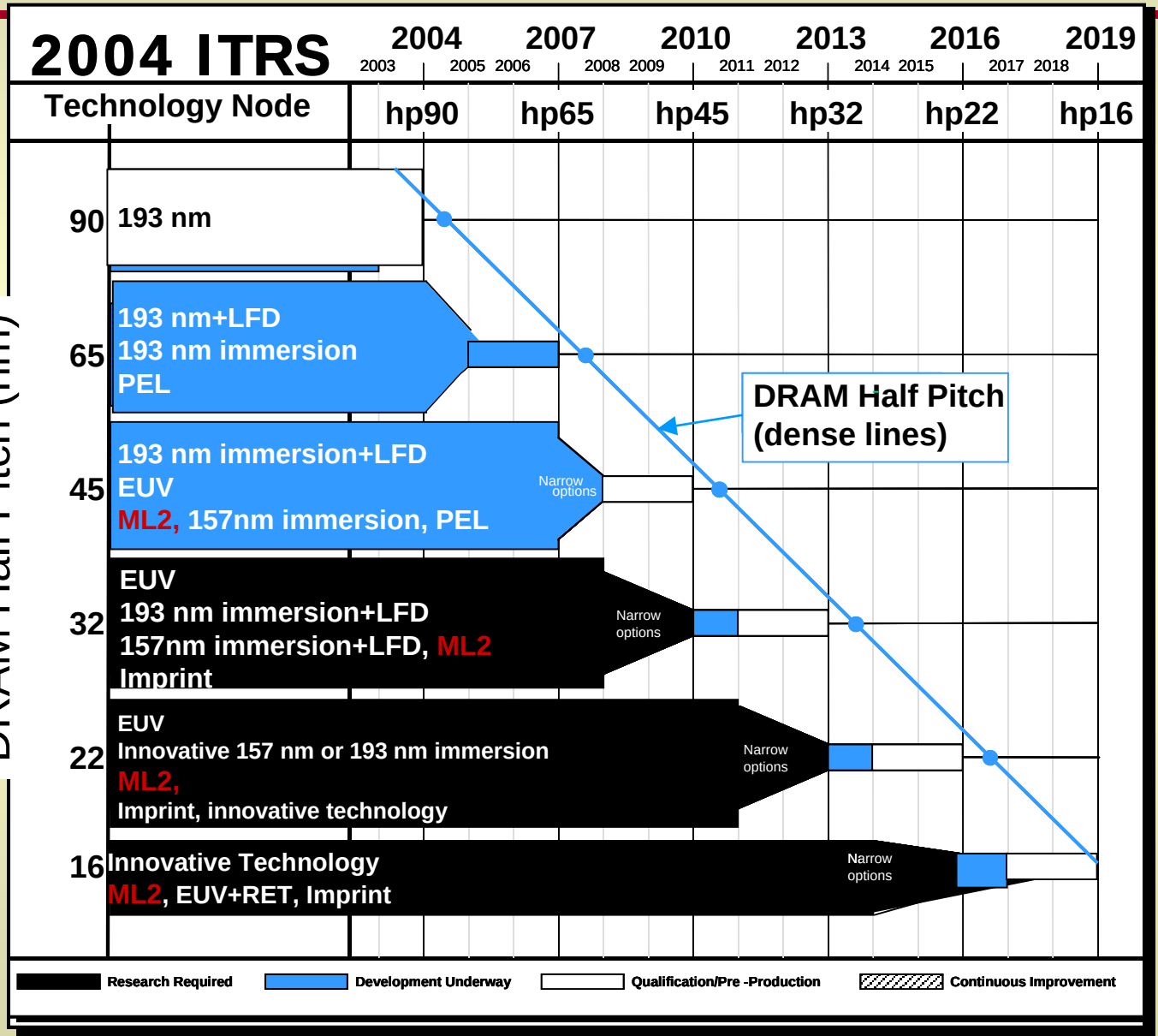
The concept to commercialization timing gap

Evolution of the SRC/DARPA Maskless Initiative

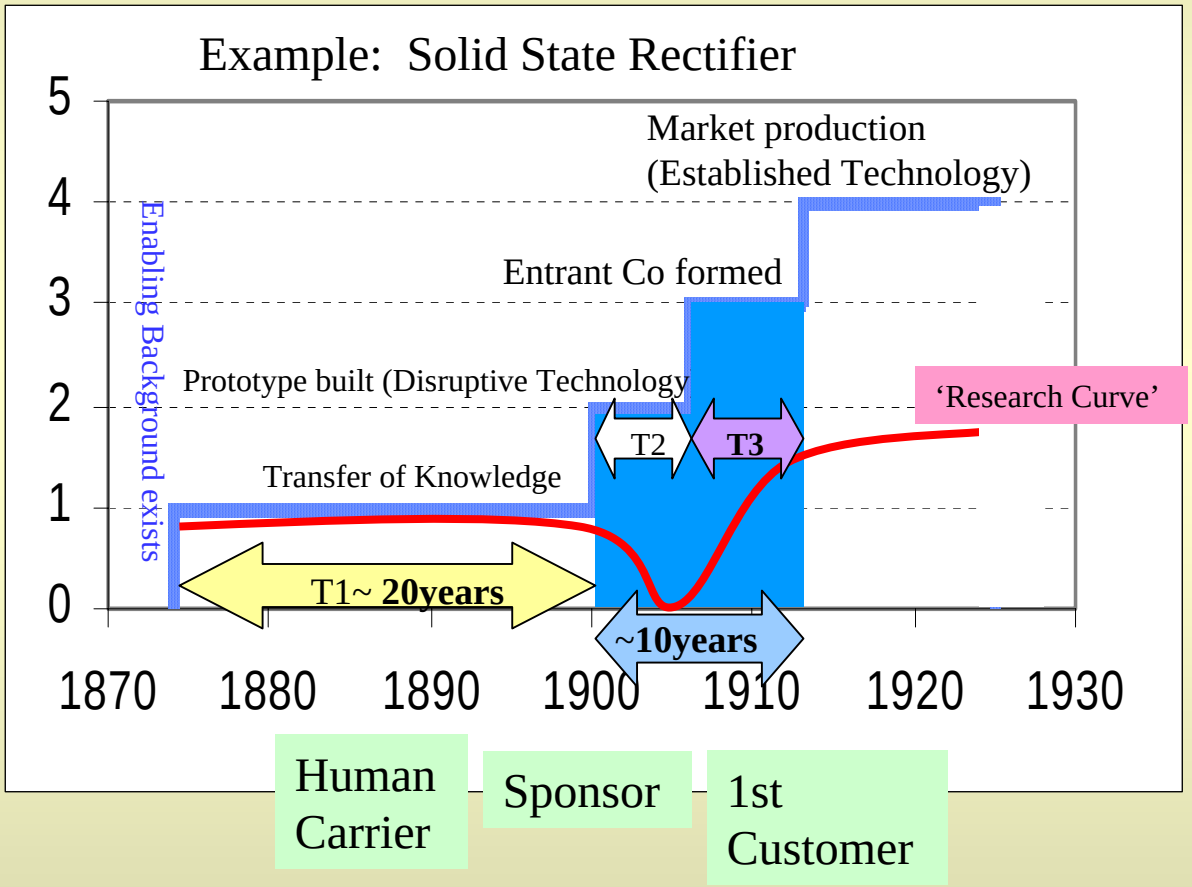
Interface of the SRC/DARPA Patterning Network with the DARPA Maskless Demonstration Project

Summary

Potential Exposure Tool Solutions



Concept to Commercialization Gap



Solid State Diode
T1 26 (1874-1900)
T2 7 (1900-1907)
T3 6 (1907-1913)
Learning Period 13 years

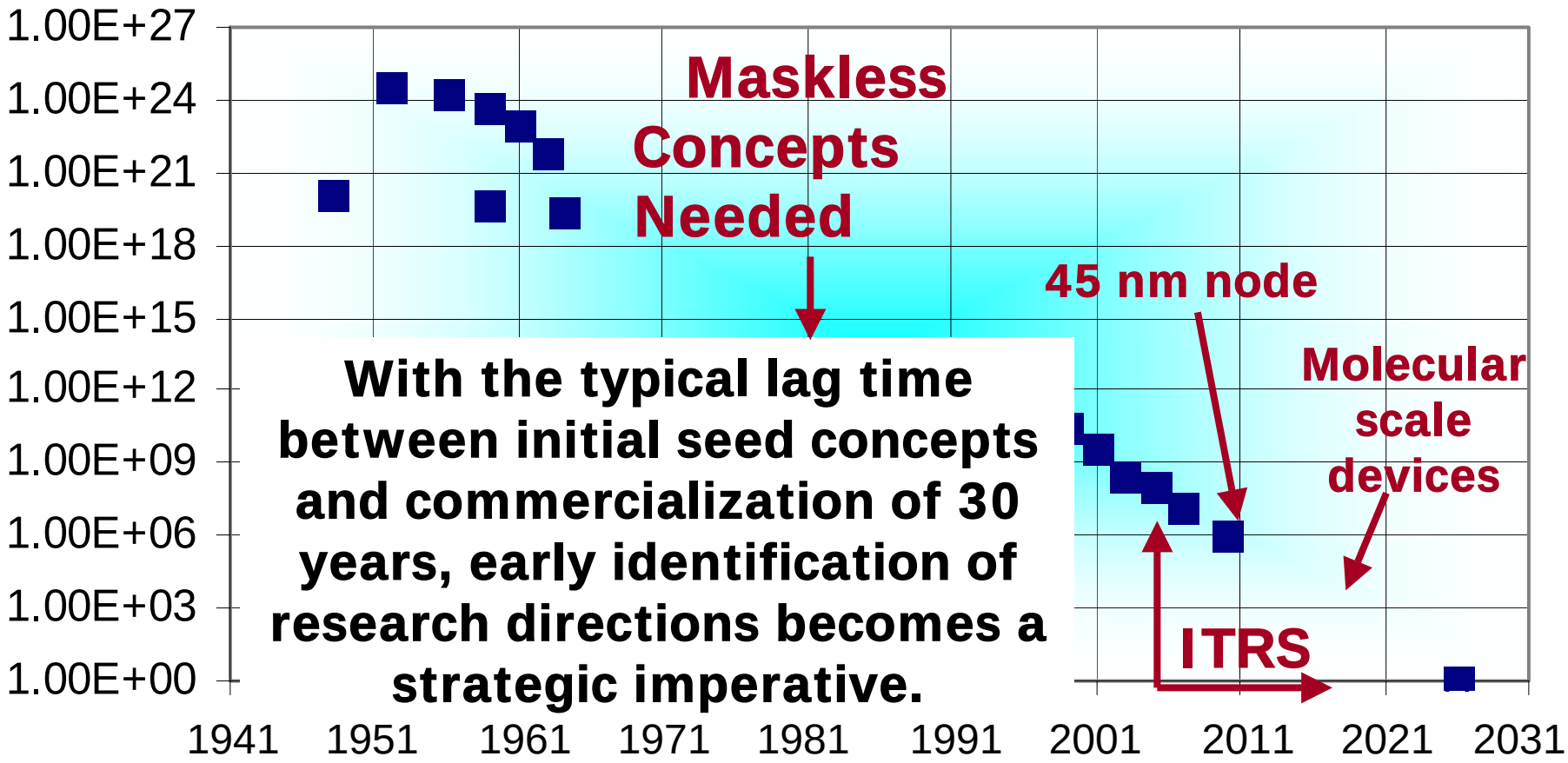
Vacuum Tube
T1 20 (1884-1904)
T2 9 (1904-1913)
T3 6 (1913-1919)
Learning Period 15 years

Transistor
T1 25 (1923-1948)
T2 6 (1948-1954)
T3 5 (1954-1959)
Learning period 11years

Integrated Circuit
T1 17 (1942-1959)
T2 3 (1959-1961)
T3 5(1961-1966)
Learning Period 8 years

Devices soon will be on the molecular or atomistic scale

Atoms per Bit



Revised from: D. Herr and V. Zhirnov, Computer, IEEE, pp. 34-43 (2001).

First Reports of E-Beam Arrayed Lithography

1. S.P. Newberry, Proceedings of the Fall joint Computer Conference AFIPS, **29**, (Sparton, Washington D.C., 1966), p. 717.
2. C.Q. Lemmond, E.C. Buschmann, T.H. Klote, Jr., and G.M. White, IEEE Trans. Electron Devices, **21**, 598, (1974).
3. D.E. Speliotis, D.O. Smith, K.J. Harte,and F.O. Amtz, Proceedings of the ELECTRO/76, IEEE, pp. 33- ?3 (1976).
4. J. Trotel, Proceedings of the International Conference on Microlithography, Amsterdam, 30 September – 2 October 1980, p. 111.
5. K.J. Harte, U.S. Patent No. 4,142,132 (27 February 1979).
6. D.O. Smith and K.J. Harte, J. Vac. Sci. Technol., **19**(4), pp. 953-957 (1981).

First Reports of Arrayed Optical Projection

- Larry Hornbeck, Texas Instruments, 1977
  - Early Piston Mirror Arrays

- Larry Hornbeck, Texas Instruments, ~1987
  - Early Tilt Mirror Arrays.
  - (Some government support in the late 1980's)

- Texas Instruments Commercialized Mirror Array Projection Technologyin the Mid-1990's.

SRC Maskless Patterning
Seed Research: mid-’80s - 1996

MacDonald, Noel	**Cornell University**
Smith, Henry	**MIT**
Frechet, Jean J.M.	**Cornell University**

- **Fast imaging materials**

SRC/DARPA Maskless Lithography Initiative: Post NGL Research Vectors

SRC/DARPA Lithography Network for Terascale Electronics (1996-)

Scanning Probes: Demonstrate lithographic patterning with large arrays of probes scanning simultaneously, demonstrate durability of tips

Multiaxis E-beam: Determine limits and performance potential of several novel approaches including multi-column shaped-beam, and NEA photocathode arrays

EUV: Demonstrate viability of fabrication approaches, mechanical and thermal viability of sub-micrometer **mirrors** using both deflection and phase-modulation approaches

Droplet-on-Demand: Determine limits and performance of drop-on-demand jet printing and investigate applications to low-cost electronics

Data Path and Circuitry: Analyze tradeoffs in compression efficiency and on-chip decoding complexity and estimate feasibility circuit complexity as limited by space and power dissipation.

SRC/DRAPA Lithography Network:
Maskless Lithography Research Team 1996 –

BOKOR,JEFFREY	Univ. of California/Berkeley
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MCCORD,MARK	Stanford University
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QUATE,CALVIN F.	Stanford University
SMITH,HENRY I.	Mass. Institute of Technology
SOLGAARD,OLAV	Stanford University
SUBRAMANIAN,VIVEK	Univ. of California/Berkeley
WILLSON,GRANT	Univ. of Texas/Austin
ZAKHOR,AVIDEH	Univ. of California/Berkeley

“Direct-Write” Maskless Lithography

Excerpt from The 2001 SRC Summer Study and the August 2001 SRC/Sematech Maskless Workshop

What *is* maskless lithography?

Pattern generation on the wafer

How?

Typically viewed as e-beam turf: “EBDW”

Many proposals for multi-e-beam wafer writers as well as cell projection

But there are many other possibilities - the key is *massively parallel arrays* of writers

When?

Minimum of 5-7 years to beta tool [2006-2008]

DARPA Low Volume Patterning Workshop September, 2003

Workshop Objectives:

- Assess optical mirror-array technology
- Determine feasibility of a demonstration project targeting:
  - 45 nm node and beyond,
  - Low Volume Patterning 1-6 W/H (300 mm)

Motivation for the Workshop

To provide value to the SRC and DARPA community
by facilitating a path to commercialization
in an area of jointly funded DARPA and SRC research
[SRC BoD authorization secured on 3/17/03]

SRC/DARPA Workshop Outcomes

- **Achieved Workshop objectives and a non-binding recommendation that DARPA proceed with a demonstration project, targeting 45 nm node and beyond**
  - **Significant technical challenges identified, but no show-stoppers apparent**
- **Identified possible benefits: superior image quality, pre-write image verification, reduced cost for low volume**
- **Identified concurrent long-term research areas**
- **Recommended close interaction with ASML/Micronic**
- **In September, 2003, DARPA issued BAA #03-42 directed to sub-50 nm maskless approaches with awards to be made in early 2004**

Critical Issues

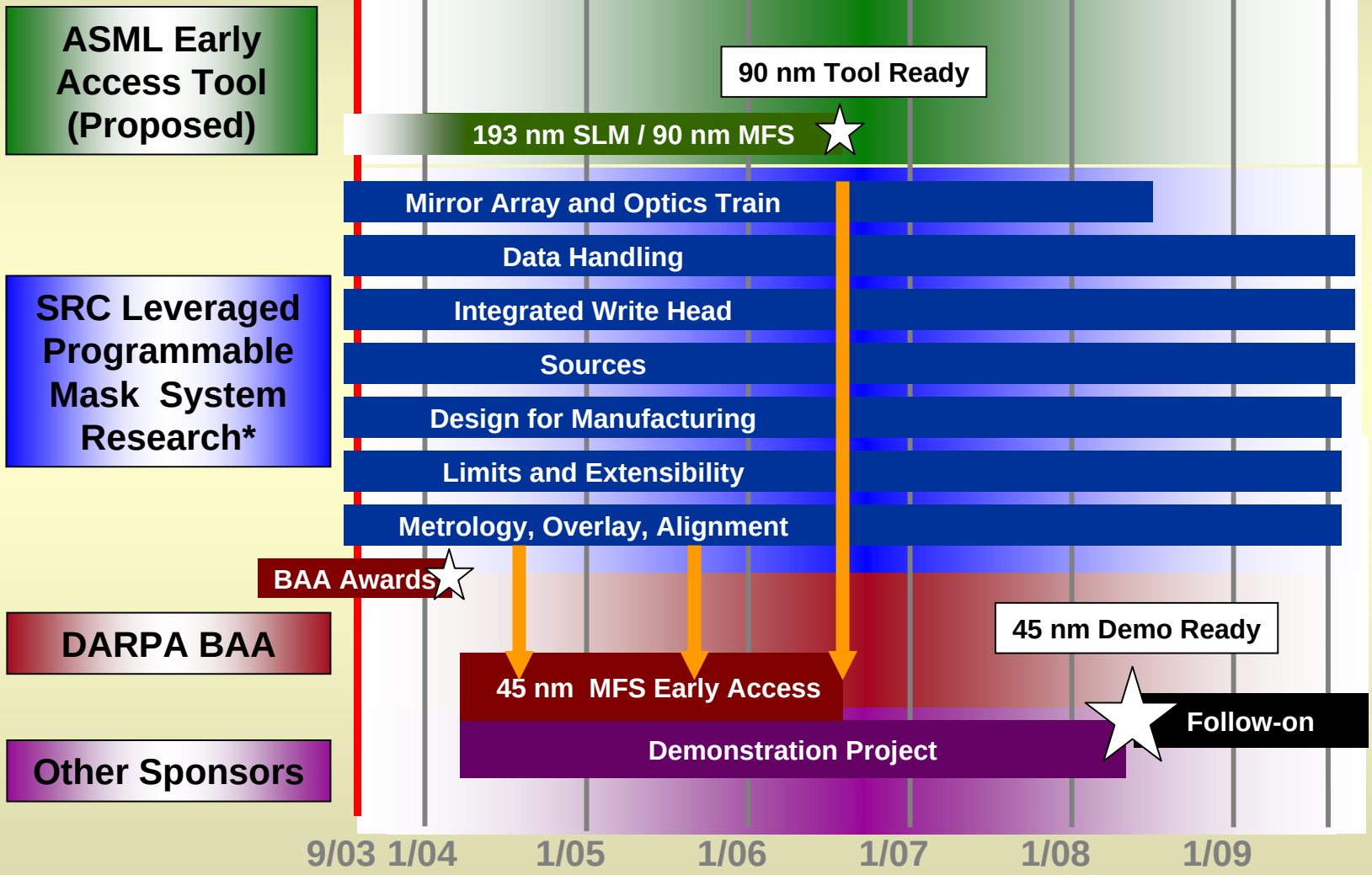
Technical challenges

For an optical approach, highest priorities include mirror-arrays and data handling

Design for manufacturability

Co-optimization with chip design ie. restricted layouts advantageous

Low Volume Patterning Demo Timeline



* In 2004, SRC and DARPA renewed their joint research commitment

Summary

In 2004, SRC and DARPA renewed their joint commitment to support maskless lithography research towards a high volume solution.

- SRC seeks partners to continue critical mass beyond 2006

DARPA BAA 03-42, Lithography for Advanced Military Systems, appears to be on track to deliver a low volume 45 nm. maskless patterning demonstration tool in 2008

- Additional external support will be needed

A high volume, 45 nm. maskless tool* may require an additional three to five years of research to develop.

* 30-60 wafer/hour

Thank You