

# ***Current Status of Polished LTEM Substrate at AGC***

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# Current Status

<p>CTE</p>	<p>Mean and spatial variation of CTE are found to be controllable. CTE dependence on temperature is also controllable. AGC will establish the production technology in the first half of 2006.</p>	
<p>Flatness</p>	<p>AGC has demonstrated the capability to achieve flatness less than 50nm by using the in-house surface figuring tool. AGC is currently concentrating to apply this tool as a HVM tool.</p>	
<p>Defects</p>	<p>AGC has been focusing to reduce pits within a polished substrate. Pits free (&gt;60nm) can be feasible. Our current best data shows defect density of 0.01 at 60nm without pits on backside chrome coated substrate.</p> <p><b>Issue; Availability of inspection tool for &lt;30 nm PSL .</b></p>	

# Implementation Schedule

Year		2004	2005	2006	2007
CTE (ppb)	Mean	+/- 15	+/- 5	+/- 5	+/- 5
	Spatial	+/- 6	+/- 6	+/- 5	+/- 5
Flatness PV (nm)		100	50	50	50
HSFR rms (nm)		0.15	0.15	0.15	0.15
Defect (/cm <sup>2</sup> )		0.05 @150nm	0.01 @60nm	0.005 @60nm	<0.0025 @60nm
Implementation Schedule		Experiment			Volume Production
		Pilot Production			