EUV Mask Blank

- **Customer's needs**
  - Defect free mask blank
    - » Blank defect density <0.003 def/cm^2 @25nm PSL (SEMI P38)
      - Commercially available: 100+ def/blank @80nm PSL
    - » Defect free blank essential for mask fabrication and wafer print
  - 30nm P-V front side flatness (SEMI P37)
    - » 12nm wafer overlay requirement (ITRS 2004 update)
      - Commercially available: ~200nm P-V front
    - » How much overlay error budget can mask have? 4-6nm?
  - High performance of multilayer
    - » Material selection of capping layer significantly impacts
      - Mask process complexity
      - Mask lifetime (oxidation, # of cleans)

SEMATECH EUV Mask Blank Roadmap and Improvement in 2004

Q3 2002 version

Year	2003		2004		2005		2006		2007		Production
Half	H1	H2	H1	H2	H1	H2	H1	H2	H1	H2	45nm
Parameter	Pre-a	Pre-a	alpha	alpha	beta	beta	beta	beta	beta	beta	gamma
Mask Substrate											
Material	LTEM	LTEM	LTEM	LTEM	LTEM	LTEM	LTEM	LTEM	LTEM	LTEM	LTEM
Mean CTE (± ppb/ deg K)	30	30	25	25	20	20	15	15	10	10	± 5
CTE Spatial Variation (± ppb/ deg K TIR)	10	10	10	10	8	8	8	6	6	6	6
Flatness Front (μm) (P–V)	0.6	0.6	0.5	0.4	0.3	0.3	0.2	0.2	0.1	0.05	0.03
Flatness Back (μm) (P–V)	1.0	1.0	0.8	0.8	0.6	0.5	0.4	0.3	0.2	0.1	0.05
Maximum Wedge Angle (μradians)	200	200	200	200	150	150	150	150	100	100	100
Surface Finish											
MSFR (nm rms)	< 2.0	< 2.0	< 1.5	< 1.0	< 1.0	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
HSFR (nm rms)	0.25	0.25	0.25	0.20	0.20	0.20	0.20	0.15	0.15	0.15	< 0.15
Local Slope of Front Surface (mrad)	N.A.	N.A.	≤ 2.0	≤ 2.0	≤ 1.5	≤ 1.5	≤ 1.5	≤ 1.5	≤ 1.0	≤ 1.0	≤ 1.0
Total Blank Defects											
Total ML Defect Density (defects/cm^2)	2.0	1.0	0.8	0.6	0.4	0.20	0.12	0.08	0.03	0.01	0.003
Cut-off Size (PSL equivalent, nm)	150	150	120	120	90	90	60	60	40	40	25
Multilayer Performance											
Peak Reflectivity (%)	>58	>58	>60	>60	>62	>62	>64	>64	>66	>66	> 67
Peak Reflectivity Unif. (%P-V) Absol.	0.80	0.80	0.70	0.60	0.60	0.55	0.55	0.50	0.50	0.50	0.50
Mean Centroid λ of Reflectivity (nm)	13.40	13.50	13.50	13.50	13.50	13.50	13.50	13.50	13.50	13.50	TBD
Centroid Reflected λ Uniformity (nm P-V)	0.08	0.08	0.08	0.08	0.07	0.07	0.07	0.07	0.06	0.06	0.06

- Supplier Performance Capability (Q3 '02) (green)
- Meet w/ upgraded tooling & process (yellow)
- New tooling / process needed (orange)
- New Tooling & Process innovation needed (red)

SEMATECH EUV Mask Blank LITH141 Project 2004 Year-end report

Efforts on Defect Reduction at Intel

- Engagement with blank suppliers
  - Blank order and regular evaluation
  - Technical information exchange on defect and surface finishing analysis
- Infrastructure development
  - EUV mask pilot line started in 2004
    - » Addressing critical areas for manufacturability
    - » Providing test masks for the EUVL program
  - Specific process modules development
    - » Modules in place: blank defect inspection, flatness measurement, absorber film deposition, dry etch, patterned mask defect inspection, defect repair and EUV reflectivity measurement
    - » Tool coming : EUV mask cleaner and reticle imaging microscope (RIM)
- Defect printability study
  - Modeling
  - Programmed defect mask fabrication and defect printing
  - Defect mitigation and compensation demonstration
- Mask handling and shipping investigation

Key Messages

- Significant improvement on EUV mask blank defect reduction has been made by the suppliers and Sematech
- Meeting blank defect requirement of 0.003 def/cm^2 @25nm is still the biggest challenge for success of EUV mask technology
- Intel continues to be actively involved in defect reduction efforts by engaging with blank suppliers and establishing in-house capability