

AMTC panelist for panel discussion No. 3 “The Mask”

Highlight

A baseline EUV mask fabrication process capable of meeting the specifications required for the set up of the ASML alpha-demo tool was established. Major improvements are required to meet high volume manufacturing specifications for the 32nm node.

Evaluating EUV mask process



- Blank material can be patterned and decent patterning performance can be achieved already now.



- CD control, registration and LER → Not specific to EUV but still a challenge for the 32nm node
- Reduction of mask defects. → Need for mask defect inspection capability.
- Reduction of blank defects. → Need for blank inspection capability.
- Mask cleaning. Not yet proven down to the required defect size.

Special items concerning SEMI P37/38

- We need to minimize the amount of stack options to allow focused blank and mask process optimization for the 32nm node.
- Define quality areas for patterning explicitly.
- So far only absorber binary mask types are covered by SEMI → Do we need other types of masks beyond 32nm?