

EUV Patterned Mask

- **Customer Expectations:**
 - » **CD's are within specification**
 - » **Layer-to-layer registration within specification**
 - » **No printable defects from:**
 - **Multilayer**
 - **Pattern**
 - **Contamination**

EUV Mask Improvement Roadmap

Parameter	Current Status	Alpha (2005)	Beta (2007)	Gamma (2009)	Node or EUV Issue?
		Spec.	Spec.	Spec.	Development Risk vs 193
Mean CTE (\pm ppb/ $^{\circ}$ K)	10	20	10	5	EUV
CTE Spatial Var. (+ ppb/oK TIR)	10	10	8	6	EUV
Flatness Front (μ m) (P-V)	85nm (best) 130nm (routine)	150	85	30	EUV
Flatness Back (μ m) (P-V)	135nm (best) 180nm (routine)	200	100	50	EUV
HSFR (nm rms)	0.10 (best) 0.13 (routine)	0.25	0.2	0.15	EUV
Local Slope of Front Surface (mrad)	2.4 (best) 5.0 (routine)	5	3	1.8	EUV
Added ML D.D. (defects/cm ²)	0.005 (best) 0.050 (routine)	0.05	0.01	0.005	EUV
Total ML D.D. (defects/cm ²)	0.23 (best) 0.80 (routine)	0.3	0.03	0.003	EUV
Cut-off Size (PSL equivalent, nm)	70nm (ML) 60nm (subst.)	80	40	25	EUV
Peak Reflectivity (%)	65.0 (best) 63.5 (routine)	>63.0	>65.0	>67.0	EUV
Peak Refl. Unif. (%P-V) Absol.	0.06 (best) 0.40 (routine)	< 0.90	< 0.70	< 0.50	EUV
Median Central λ Offset (nm)	0.00 (best) 0.04 (routine)	< \pm 0.09	< \pm 0.075	< \pm 0.06	EUV
Reflected λ Uniformity (nm P-V)	0.022 (best) 0.058 (routine)	0.08	0.07	0.06	EUV
Mask Nom. Image Size (4X)	150nm (multiple suppl)	120	100	90	Node
Mask Min Primary Size DLS(4X)	125nm (AMTC) 100nm (Intel)	100	90	89	Node
IP (nm multi.)	????	12	11	10	Node
CD Unif. DLS (nm)	11.0nm (AMTC)	11	9	7.5	Node
Absorber LER	????	5	4	3	Node
Pattern Inspection Sensitivity	65 nm	65 nm	45 nm	32 nm	Node
Contamination Removal & Inspection Capability	100 nm	65	45	32	Node
Shipping/Handling		No added defects	No added defects	No added defects	EUV

Substrate

Blank

Mask

Risk Color Code

EUV >> 193

EUV > 193

EUV = 193 or no issue

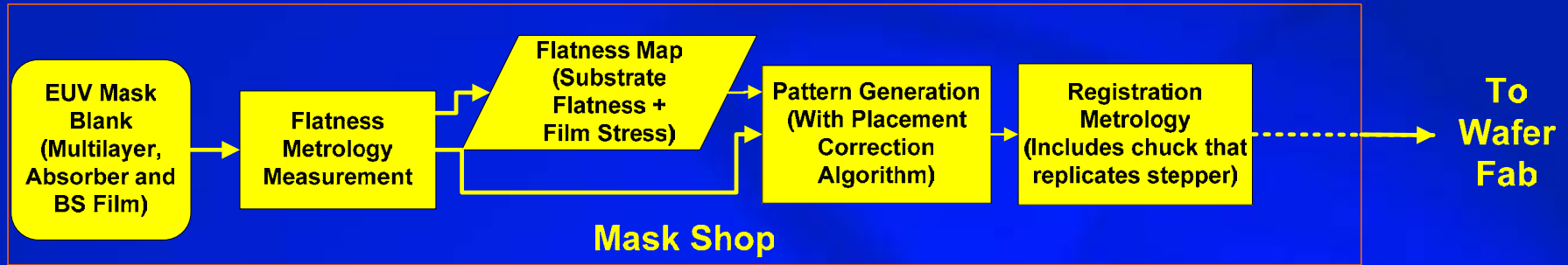
EUV < 193



EUV Patterned Mask Supplier Focus

- **Three buckets for development and risk mitigation**
 - **Technology node (independent of litho technology)—examples:**
 - » Minimum primary feature patterning capability
 - » Mask capital equipment roadmap, schedule and cost
 - **Diverging risks and requirements (litho technology dependent)—examples:**
 - » Sub-resolution patterning capability (193)
 - » CD uniformity for high MEEF structures (193)
 - » ML compatible cleaning process (EUV)
 - » Robust reflected light defect inspection (EUV)
 - **Risks and development unique to litho technology (EUV)—examples:**
 - » Multilayer defect printability
 - » Potential need for blank actinic inspection
 - » Metrology, process, and chucking for mask flatness (registration)
 - » Shipping, handling and storage without pellicles

Image Placement (Registration)



• Key Focus

- Flatness Metrology with sufficient accuracy and repeatability
- Pattern generator
 - » Correction algorithm
 - » Mask fixturing (E-chuck, 3-point, clamp etc.)
- Registration metrology with chucking option
 - » Must replicate E-chuck for validation
 - » Repeatability of chucking
- E-chuck on exposure tool
 - » Optimal E-chuck configuration
 - » Repeatability of chucking
 - » Fabrication of chucks that meet flatness requirement

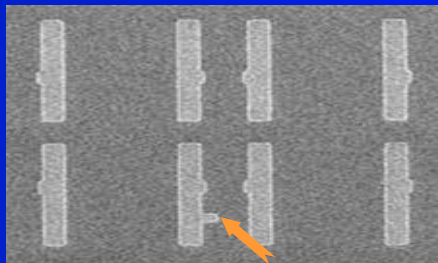
Correlation ??

• Chucking Solution Remains High Risk !

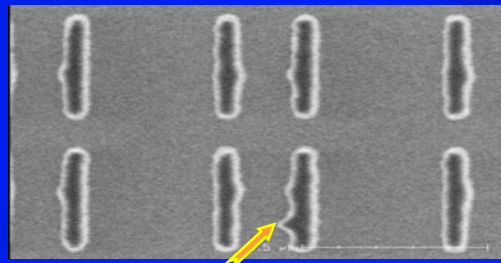
Defect Printability

- Active program using MET and Programmed Defect Mask (PDM) to assess printability
 - Measure printability by $\% \Delta CD / CD$ from mask with modeled defects
 - EUV high k1 printing with low MEEF allows scaling to 22 nm node features

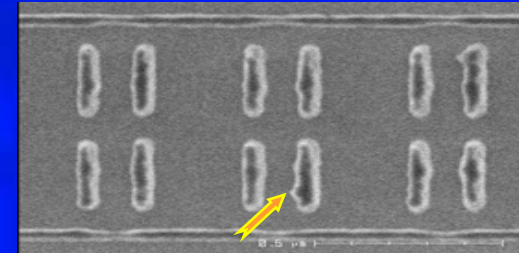
5X Mask



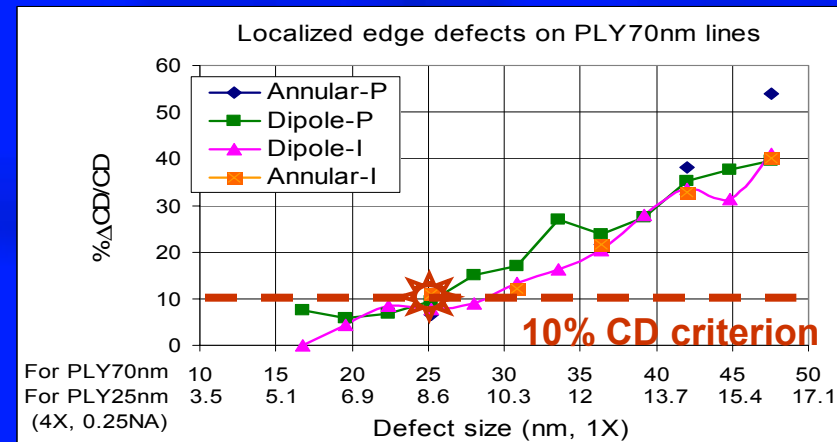
Resist 70nm PLY



Resist 50nm PLY



- Printing on MET@ Intel and MET@ ALS

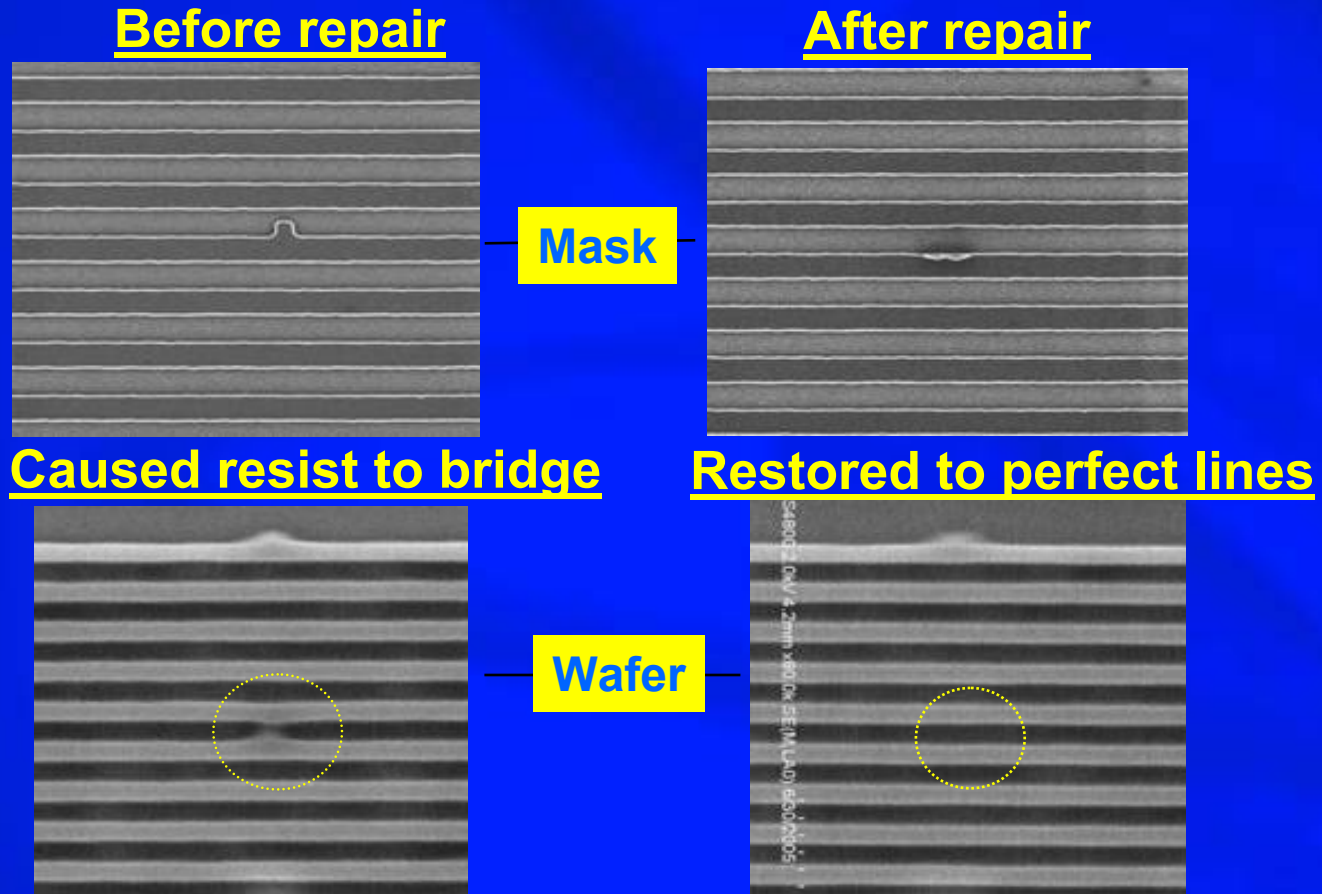


Ted Liang, Intel Components Research

Defect Repairability

- **Pattern repair with e-beam induced nano-structuring**
 - Both etch and dep process demonstrated for 32 nm node specs
 - Repair process validated by MET print test with 100% yield

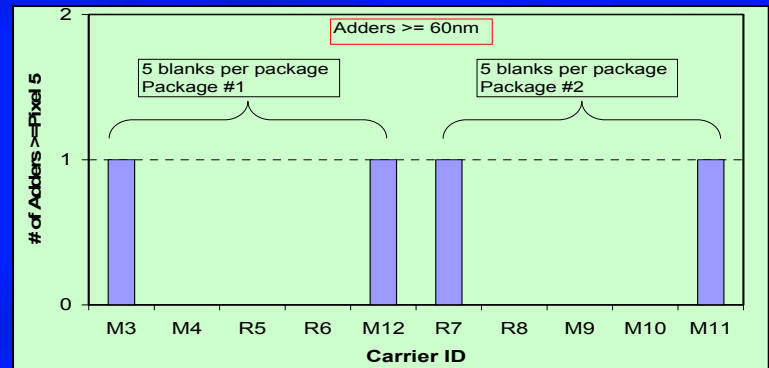
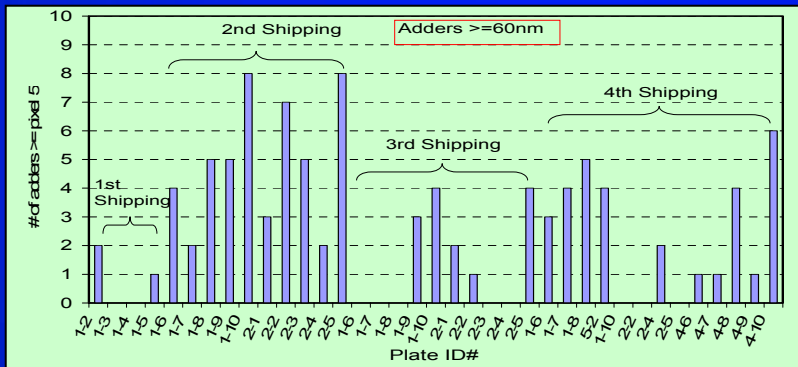
Example on 50nm L/S



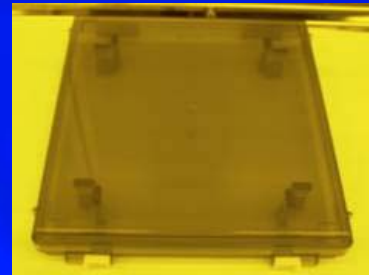
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Shipping/Handling

- **Shipping: Considerable progress on identifying a solution path**
 - Shipping experiments performed using various carriers, configurations and orientations
 - Some results using “standard” industry carriers, round trip shipping from CA ↔ NY, M1350 inspection (60 nm sensitivity) with area 145x145mm²
 - **Results:**
 - » Vertically shipping orientation: Adder range from 0 to 8 for 37 carriers (no data excluded in the shipping results)
 - » Horizontal shipping orientation, front side down (5 stack): 1 random adder = noise level of current handling/inspection protocol used in test



Pei Yang Yan, Intel Components Research



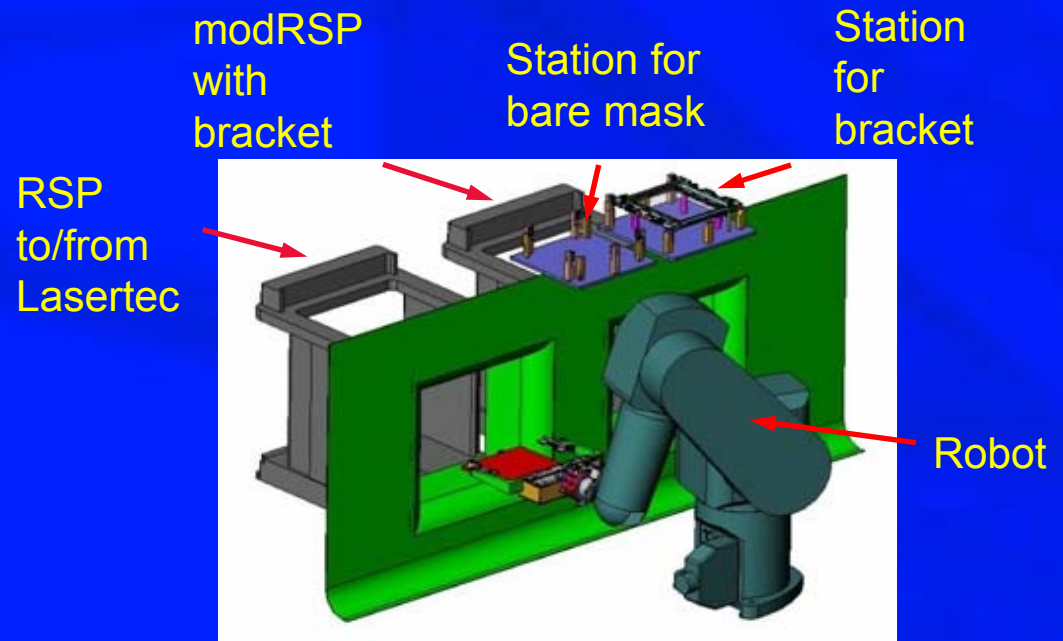
Shipping/Handling

- **Handling:**

- **Experiment performed using EUV reticle sorter at Intel. Cycle:**

1. Open RSP200 and move mask out
2. Rotate mask face down
3. Mount mask to a bracket
4. Move the bracket/mask set to the modified RSP200
5. Close the modified RSP200
6. then reverse the procedure to bring the bare mask back to its original RSP200

- **223 full cycles (about 22 hrs continue run) with total of 3 adders @ $\geq 60\text{nm}$**



Pei Yang Yan, Intel
Components Research

Summary and Key Messages

- **Partition development needs into 3 buckets**
 - Node requirement (need to do anyway)
 - Diverging requirement (make sure EUV need is comprehended)
 - Unique requirement (EUV specific)
- **EUV efforts must concentrate on unique and diverging needs—place to focus on risk reduction**
- **Good progress in many (mask fabrication) areas with an integrated solution on the horizon**
 - Defect printability methods and plan
 - Absorber repair process
 - Encouraging shipping and handling results
- **Much more to do**
- **Least progress (speaker's opinion) on demonstrating integrated image placement (registration) solution**
 - E-chuck design, fabrication and efficacy
 - Metrology and integration with pattern placement at generation
 - Correlation between exposure environment and mask placement metrology