ASML

EUV Mask Technology Workshop

Panel Session # 3 – The patterned Mask

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Panel #3 – The Patterned Mask
ASML is a “Customer” – for tooling & setup masks

- EUV mask production specs vs. current best capability
  - Need full compliance with SEMI specs:
    - SEMI P37 – Substrate: physical dimensions & properties, flatness
    - SEMI P38 – Blank: coating characteristics
  - Patterning:
    - Alignment marks, Handling (exclusion) zones
  - Handling (in tool)
    - need mask carrier solution for production
  - Transport (out of tool handling): outgassing, particles
    - need transport box solution for production

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Expectation on ITRS 32nm HP mask requirements

- Image size, CD, IP, defects
  - Image size – full field, maximize usage of the mask area
  - CD – consistent with 32nm HP node:
    - We need structures that demonstrate imaging capability consistent with the 32 nm HP node – i.e DL, IL, etc - but do not have to produce working devices
  - IP: the tolerance of the pattern versus the glass edge is < 0.2 mm in both X and Y directions
  - Defects – not so critical because
    - structures used by ASML on tool qualification and set-up reticles are repetitive (as opposed to structures needed by IC mfg’s for making devices)

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Mask Repair & Cleaning

- Mask repair & cleaning is not likely to be needed in house for tooling and set-up reticles
  - repetitive structures allow for using alternative fields
  - Multiple sets of tooling masks allow for off line repair and/or cleaning if necessary – return to mask house
  - Must qualify delivery process from mask house to ensure particle and vacuum qualification remains intact
- Mask inspection not likely to be needed in house
  - Set up tests will detect mask defects, but does not impact tests results or yield (not making devices)
  - Inspection at mask house when masks are sent back for repair and/or cleaning

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