



# ASML

## EUV Mask Technology Workshop

### Panel Session # 4 – Mask Usage

## Panel #4 – EUV Mask Usage

### ASML is a “Supplier” – of exposure tools using masks

- EUV mask production specs vs. current best capability
  - Need full compliance with SEMI specs:
    - SEMI P37 – Substrate: physical dimensions & properties, flatness
    - SEMI P38 – Blank: coating characteristics
  - Patterning:
    - Alignment marks, Handling (exclusion) zones, device structures, other special features (e.g. – flare compensation)
  - **Handling (in tool)**
    - need mask carrier solution for production
  - Transport (out of tool handling): outgassing, particles
    - need transport box solution for production

*Except for **patterning**, these are the same needs as for ASML as a “Customer”*



# Expectation on ITRS 32nm HP mask requirements

- Image size, CD, IP, defects
  - Image size – full field, maximize usage of the mask area
  - CD – consistent with 32nm HP node:
    - Must meet all the requirements of the 32nm node
  - IP: the tolerance of the pattern versus the glass edge is < 0.2 mm in both X and Y directions
  - Defects – critical
    - Impact on yield for end users
    - Exposure tools must not add defects (particulate or molecular)

*Except for **defects**, these are the same needs as for ASML as a “Customer”*

# Mask Repair & Cleaning

- Mask repair & cleaning potentially needed in fab
  - Yield loss driven by repeat defects
  - Limited sets of masks (especially in early years) likely means turnaround time for off line repair and/or cleaning by mask house is too long
  - Must qualify handling process in fab to ensure particle & vacuum qualification remains intact
- Mask inspection potentially needed in fab
  - Preventing yield loss by periodic mask inspection is already done for optical masks
  - Turnaround time for Inspection at mask house is likely to be too long