

EUV Mask Usage

- **Customer Expectation**

- **Solution for EUV mask protection from particles and contamination in the chain of mask usage**

- » **Shipping and handling**

- **System to maintain cleanliness of mask from maskshop to wafer fab**

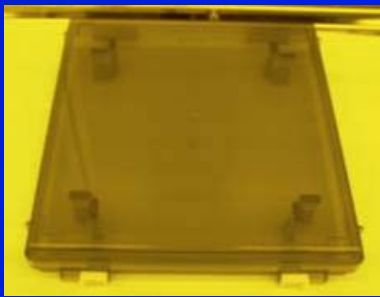
- » **Exposure tool**

- **Assurance of no added particles**

- » **Wafer fab mask storage, handling and in-fab mask cleaning capability**

Case Study and Investigation of Mask Shipping and handling at Intel

Vertical vs. Horizontal



Manual vs. auto handling



Shipping box arrangement

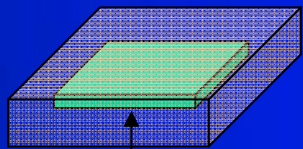


Pei-Yang Yan,
Intel Components Research

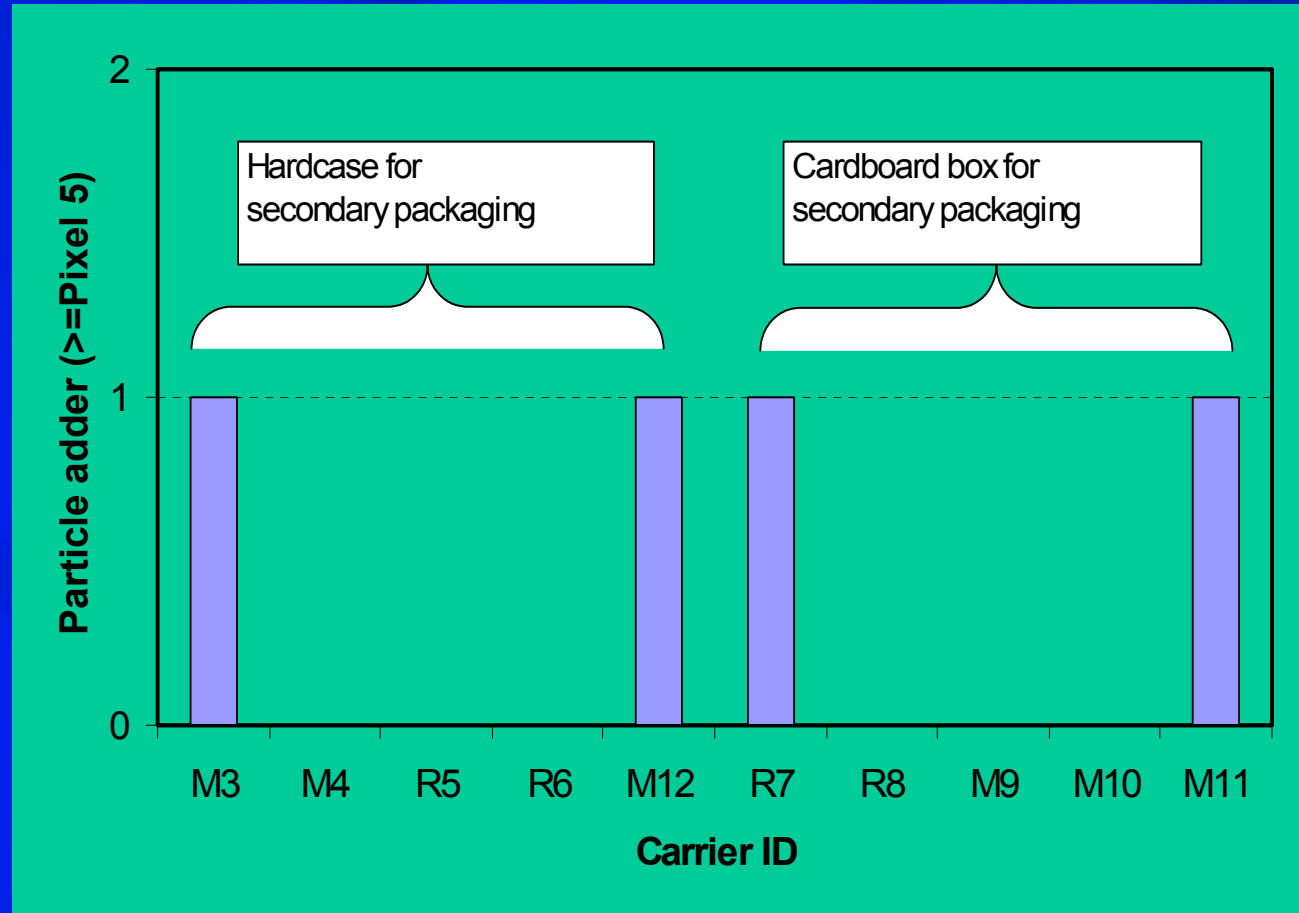


Encouraging Result of Shipping with Front Side Face Down

Round trip shipping
from SC ↔ NY
M1350 inspection
with scanned area
145mm²



Front side
facing down



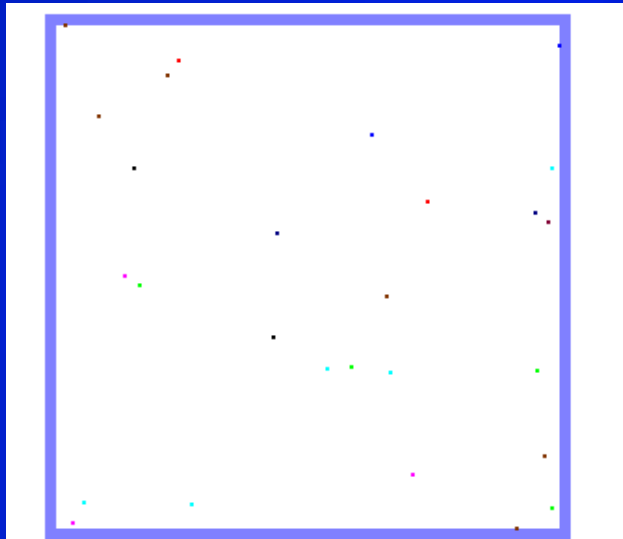
➤ 1 adder reach the noise level of the current handling and inspection protocol used for the test

Pei-Yang Yan, Intel Components Research

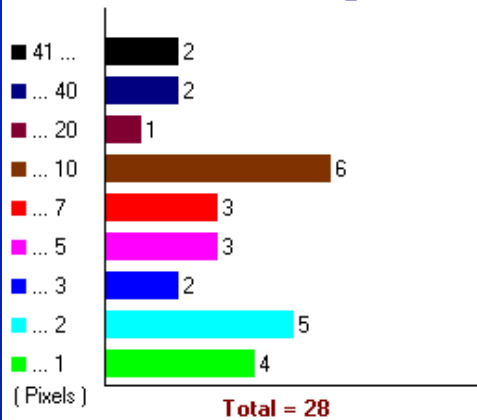


Round Trip Shipping – ID#M3: 1 adder @pixel 5

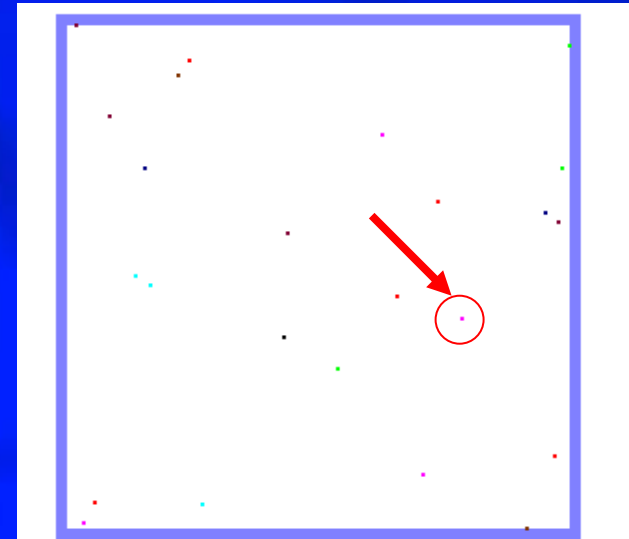
Pre-scan (area 145mm²)



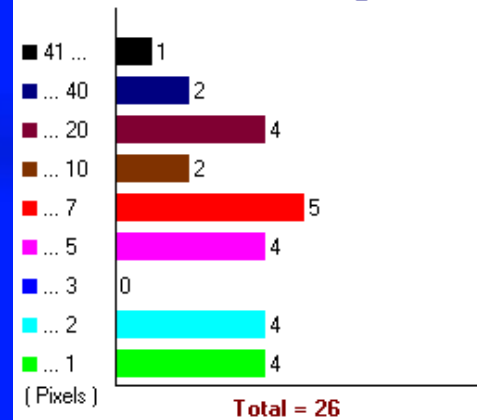
Pixel Histogram



Post-scan (area 145mm²)

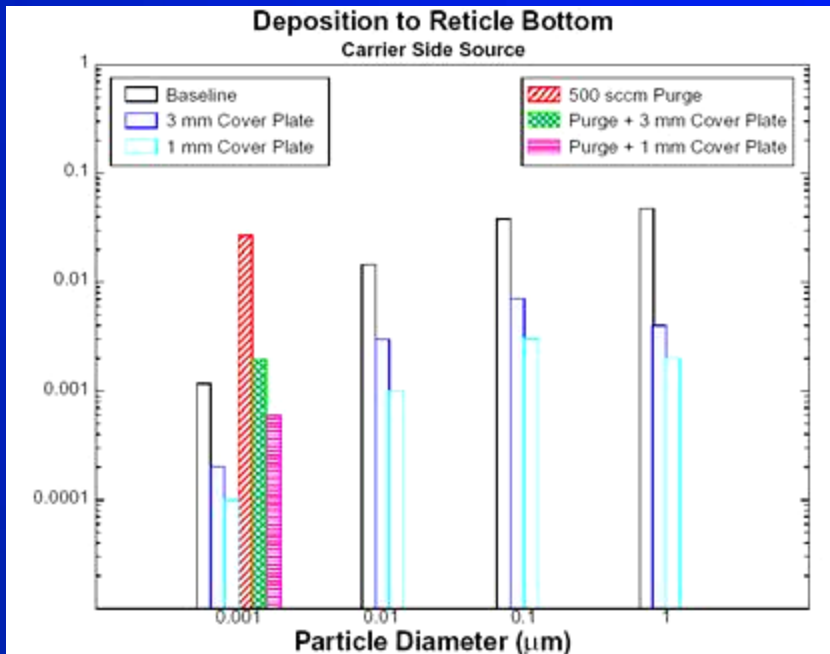


Pixel Histogram



Simulation/Experimental Verification of Cover Plate Protection

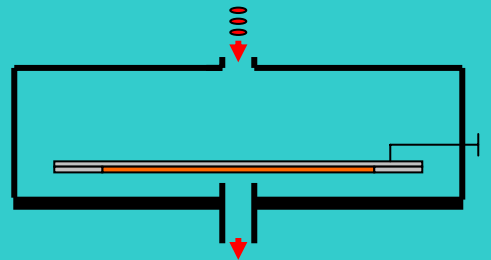
**Simulation
Sandia National Lab**



• **Low particle deposition rate for narrow cover plate gap**

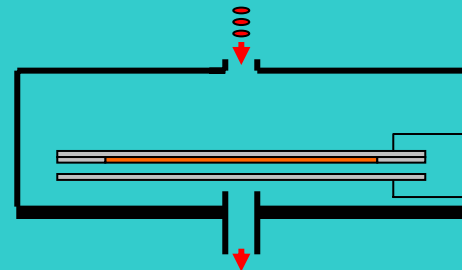
**Experiment: Zero charge particles (125nm)
(U. of Minnesota)**

Sampling = 20 min, 1.8×10^6 particles injected



No cover
2788 particles
were added

Sampling = 20 min, 1.8×10^6 particles injected



With cover
2 particles were
added

Key Messages

- **Sematech and Intel have demonstrated very low defect levels during the complex shipping and handling tests**
- **ASML has demonstrated very low defect levels in the reticle loading test in vacuum environment**
- **Intel continues to be actively involved in defect reduction efforts by engaging with carrier suppliers, collaborating with Sematech, and conducting in-house development**