



Intel presentation to Semi-standards task force

Suggestions and things to consider

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11/10/05



Overview

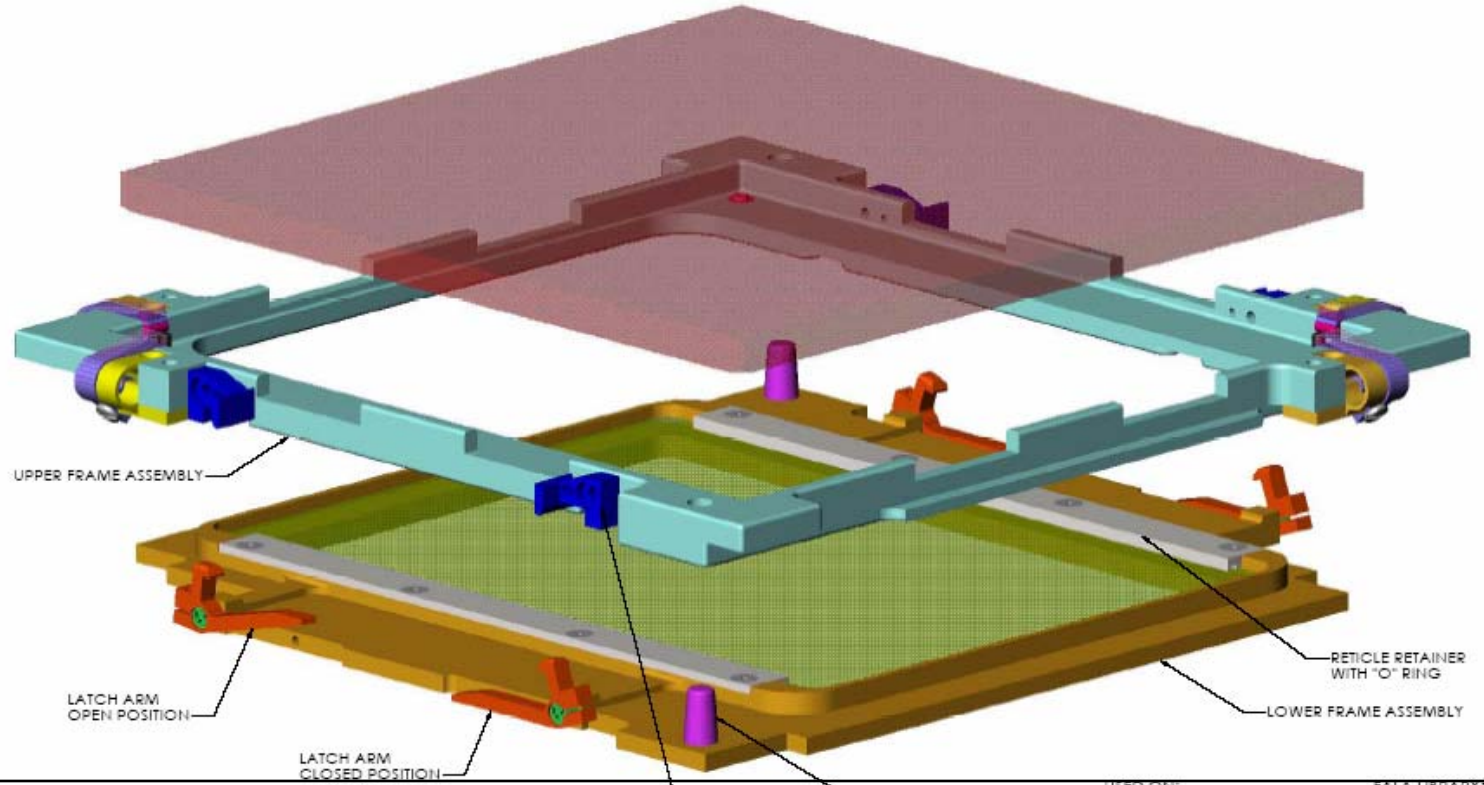
- ❖ **Intel suggests considering two mask carrier standards:**
 - * In fab carrier – current focus
 - * Shipping carrier – needs equal attention

- ❖ **Possibility that the two may converge, but it may be best to separate the problem and work from there.**

- ❖ **Learn from lesson of wafer carrier Semi standards development (did not address shipping standard early on –became was a last minute solution)**



Intel Bracket Design

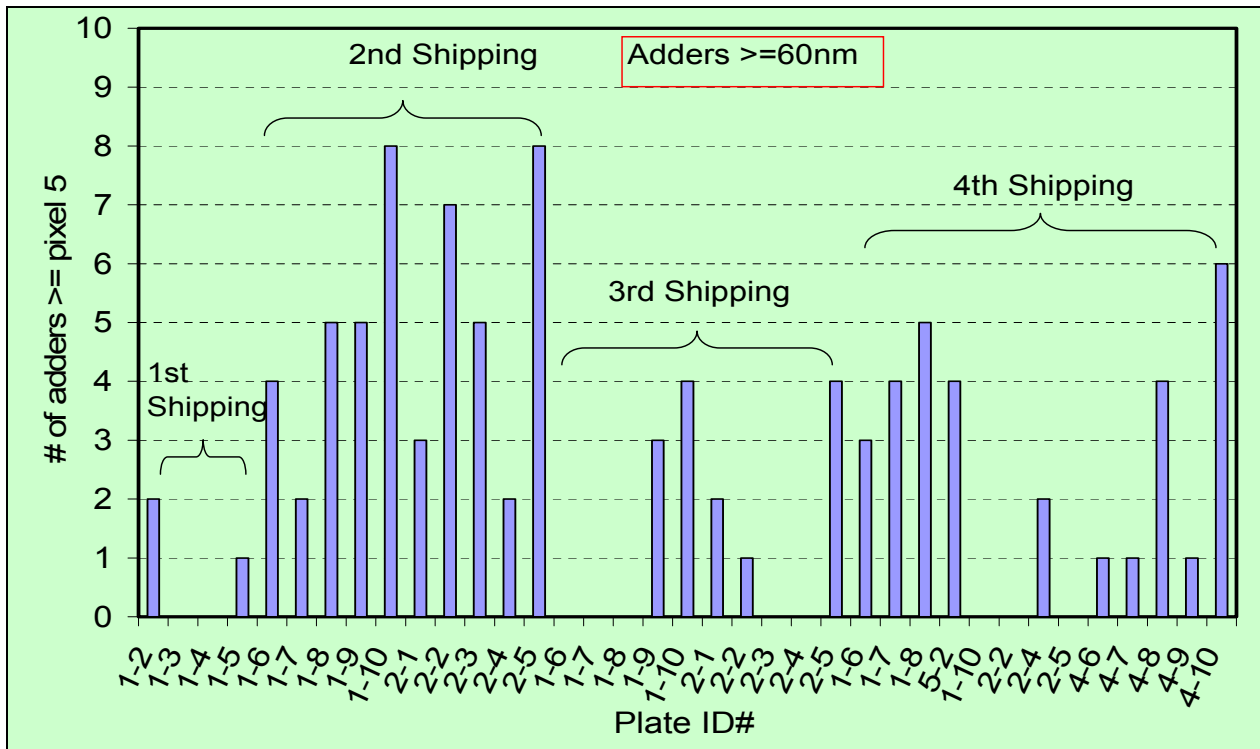


- ❖ This is only a test vehicle for data collection
- ❖ Not necessarily for manufacturing purposes
- ❖ Mask would sit face-down
- ❖ Bottom Tier serves as a removable pellicle



Reticle Shipping Test Using Intel testing Shipping Carrier (Mask carrier places Vertically during Shipping)

Round trip shipping from CA↔NY M1350 inspection with area 145x145mm²

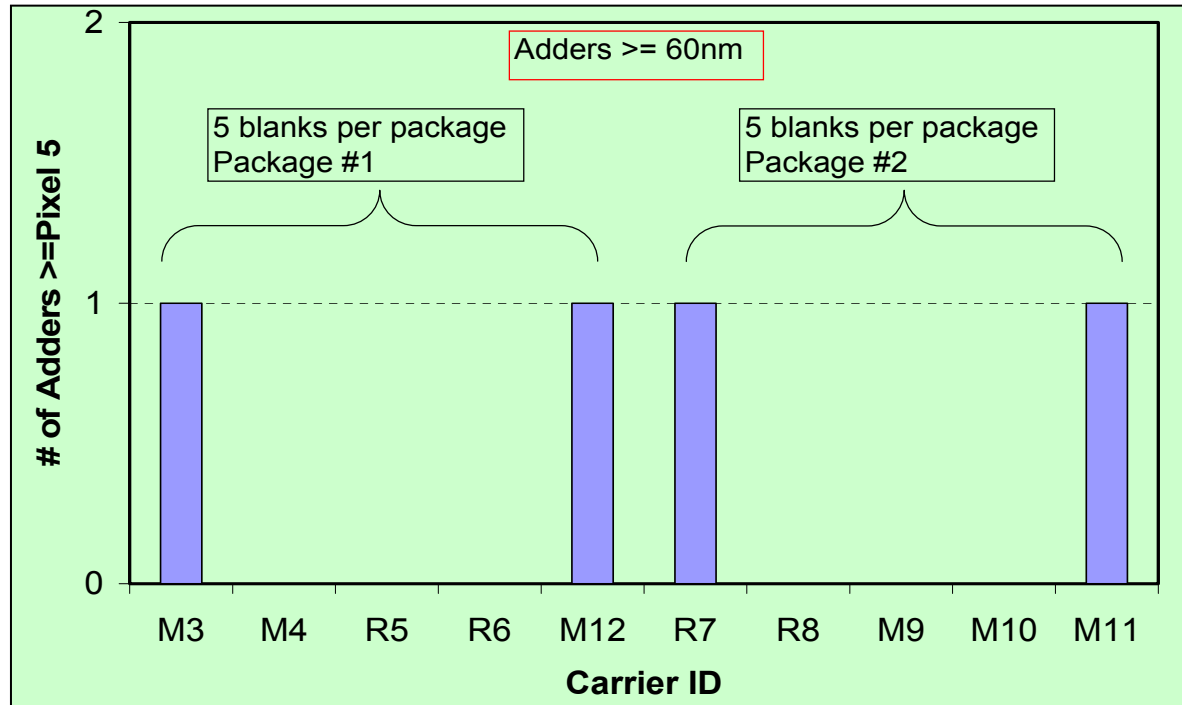


Range from 0 to 8 for 37 carriers (no data excluded in the shipping results)



Reticle Shipping Test Using Intel testing Shipping Carrier (Mask carrier placed horizontally during Shipping)

Round trip shipping from CA↔NY M1350 inspection with area 145x145mm²



- 1 random adder = noise level of current handling/inspection protocol used in test
- Mask front side down in shipping provides better protection than vertical placement



Summary and Next steps

- Mask front side facing down during shipping provided better protection over the vertical shipping arrangement**
- The shipping carrier demonstrated either zero or one particle adder with front side facing down during shipping (one adder is within the noise of handling and measurement). These are the best shipping result one can have with current best metrology**
- RH shipping test for particles ≤ 60 nm is limited by the metrology capability**
- Task Force needs to figure out how to best address the development of shipping carrier standards while also addressing in-fab carriers in parallel**