AP Regional Update

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Semiconductor Leading Edge Technologies, Inc.

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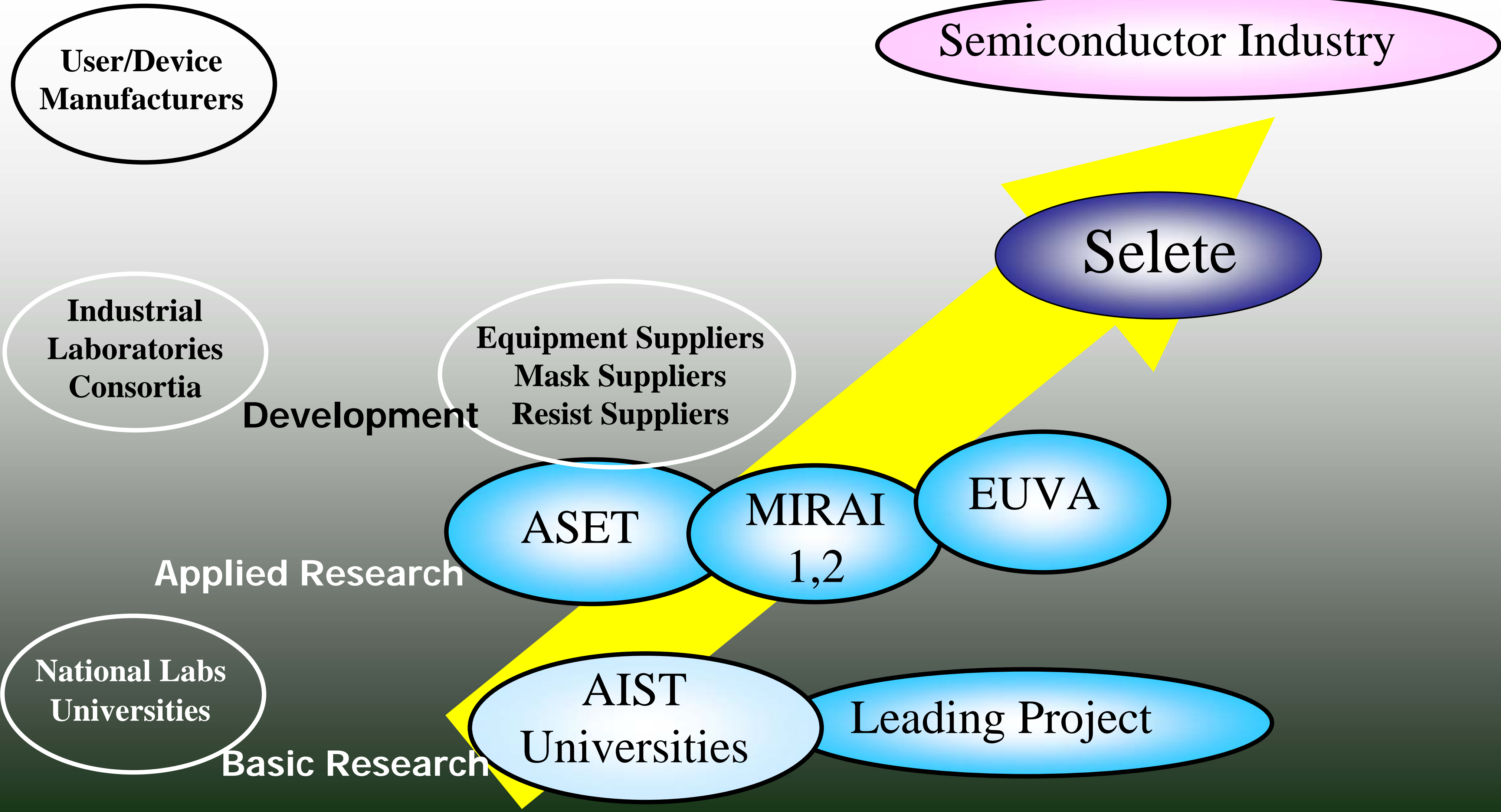
by Prof. Jinho Ahn, Hanyang University

Japan Update

- **Background:**
  - Japanese semiconductor consortia were renewed in April, 2006.
  - Selete : new organization, scheme, programs
  - Tsukuba Semiconductor Consortium (TSC) manages both Selete and MIRAI-3 project.

- **Selete started EUVL Programs in April, 2006.**

Function of Each Consortium



Shinji Okazaki, ASET-EUV

Outline of Selete EUV Programs

Selete

- 5-year program : FY 2006-2010
- Scope : Lithography integration development stage for applying EUVL to volume production
  - Accelerate key unit technology development
  - Lithography design & integration
- Funding :
  - EUV Mask Program (NEDO funded : MIRAI 3)
  - EUV Lithography & Mask Program (Industry funded)
- Member companies :

  4 device manufacturers

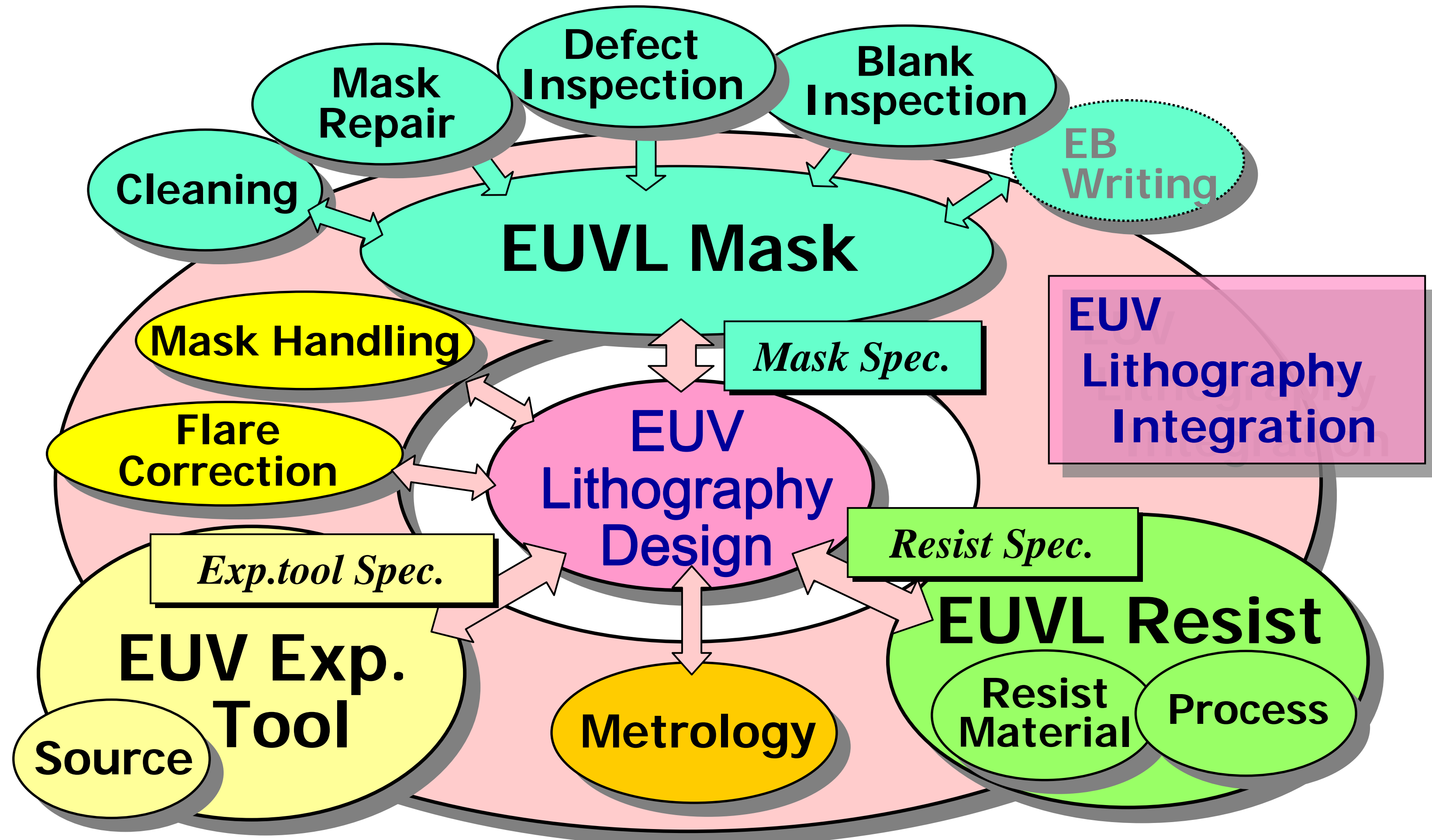
  FUJITSU, NEC Electronics, Renesas Technology, TOSHIBA

  3 Mask suppliers & 6 Tool suppliers

  TOPPAN, DNP, HOYA, CANON, NIKON, SCREEN, TOKYO ELECTRON, SOKUDO, Hitachi High-Technologies
- Cooperate with ASET, EUVA ,Leading PJ, University of Hyogo, Osaka University, Osaka Prefecture University and AIST

EUV Lithography Design and Integration

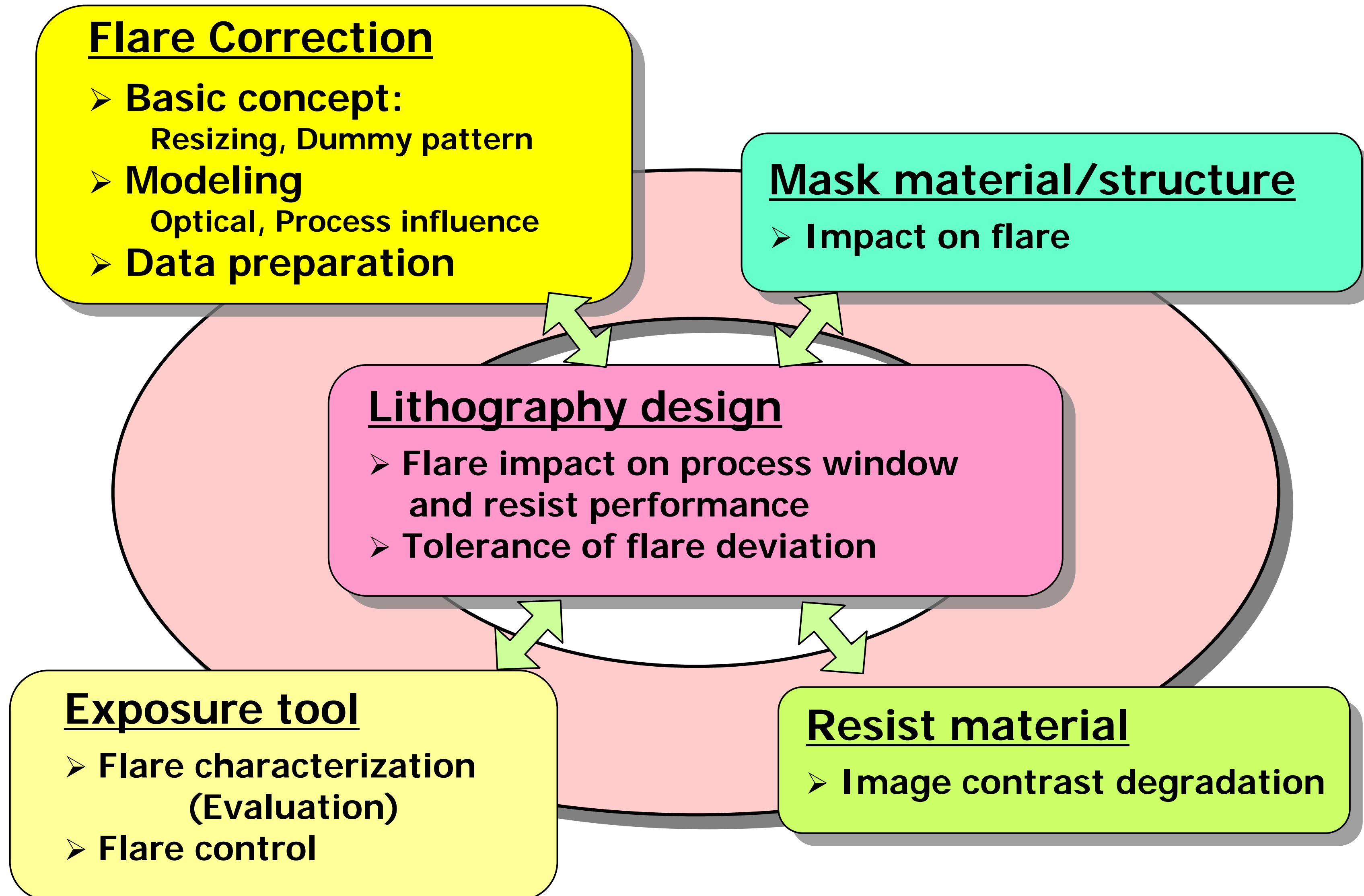
Selete



" Flare management "

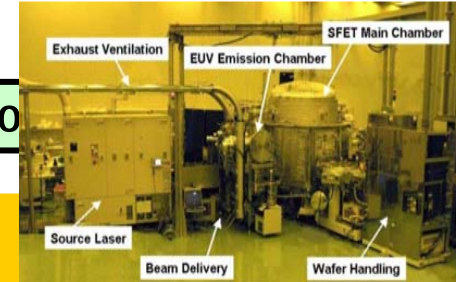
Selete

10% level flare impacts significantly lithography performance.



EUV Lithography Program

Selete



FY		06	07	08	09	10
Exposure tool		SFET (EUVA/Canon) Small Field Exposure Tool; EUV1 (Nikon) Full Field Exposure Tool				
Lithography process development		■ Exposure tool evaluation (Source/Optics lifetime, Contamination, Flare) ■ Resist materials (sensitivity, resolution, LER, out-gassing,) ■ Resist process (multilayer, coating/developing process) ■ Flare correction; Verification using FEP/BEP TEG				

32nm L/S

EUVL Mask Program (NEDO funded)

Selete

- **High quality mask and blank development**
  - **At wavelength mask and blank inspection***

    based on MIRAI-1,2 development
  - **Specifications for mask structure, materials and defectivity**
  - **Mask contamination control**
- **Mask infrastructure construction**
  - **Mask pattern defect inspection**
  - **Mask pattern defect repair**
- **Mask handling technology**
  - **Particle contamination-free mask handling without pellicle***

    Mask Protection Engineering Tool (MPE Tool)
  - **Inspection and cleaning in wafer fab**

* The recent results will be presented during the poster sessions at the symposium.

Korea Update

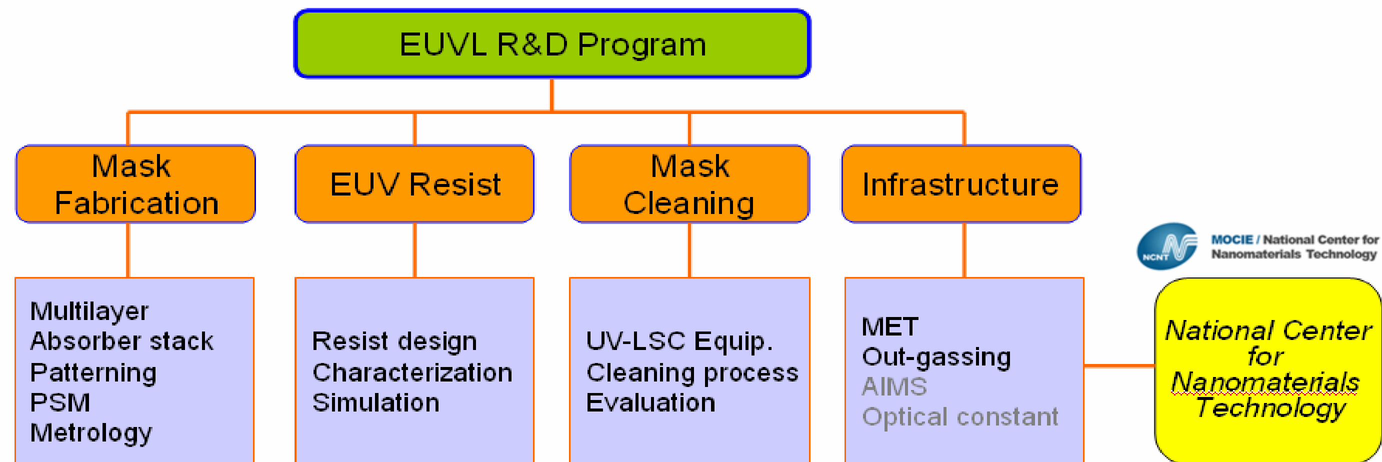
EUVL R&D Program: Dec. 2002 – Aug. 2010 (Phase 2: Sep.2005 – Aug. 2008)

Members:

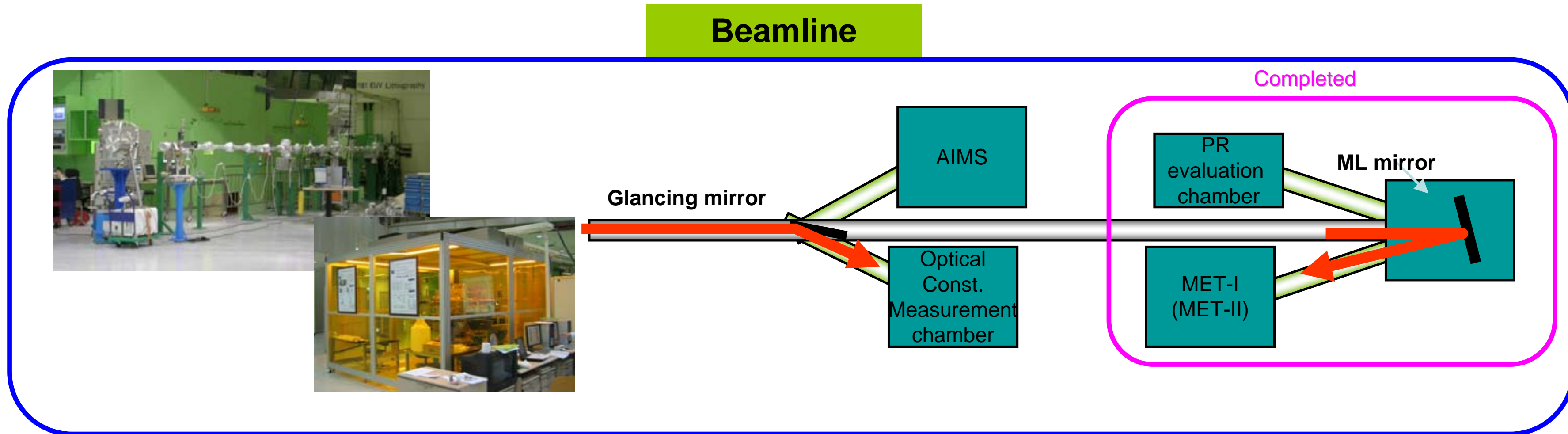
Academia - Hanyang U., POSTECH, SKKU, Inha U.

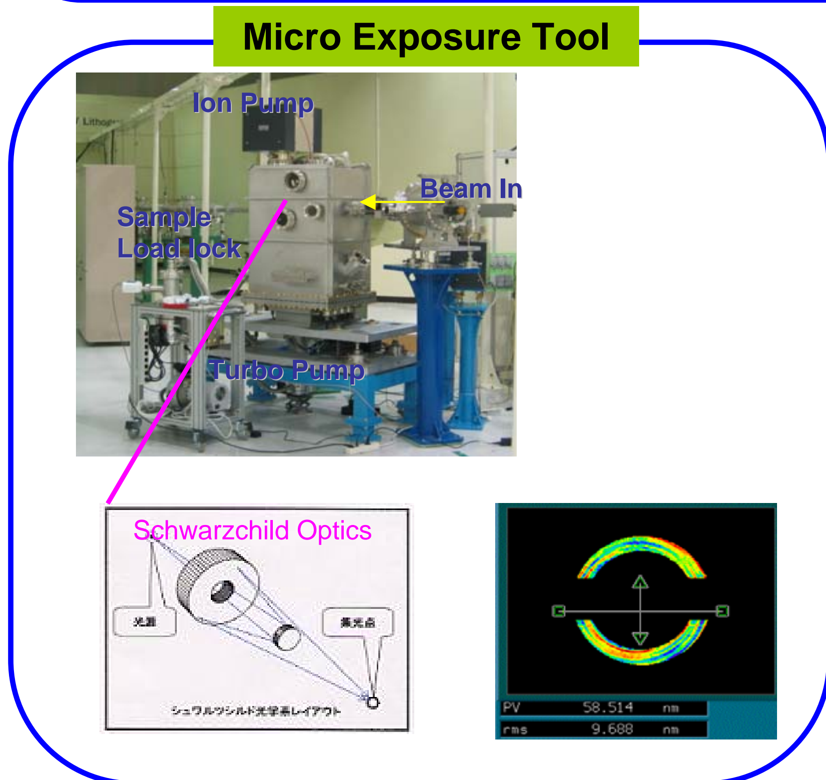
Research Institute – Pohang Accelerator Laboratory

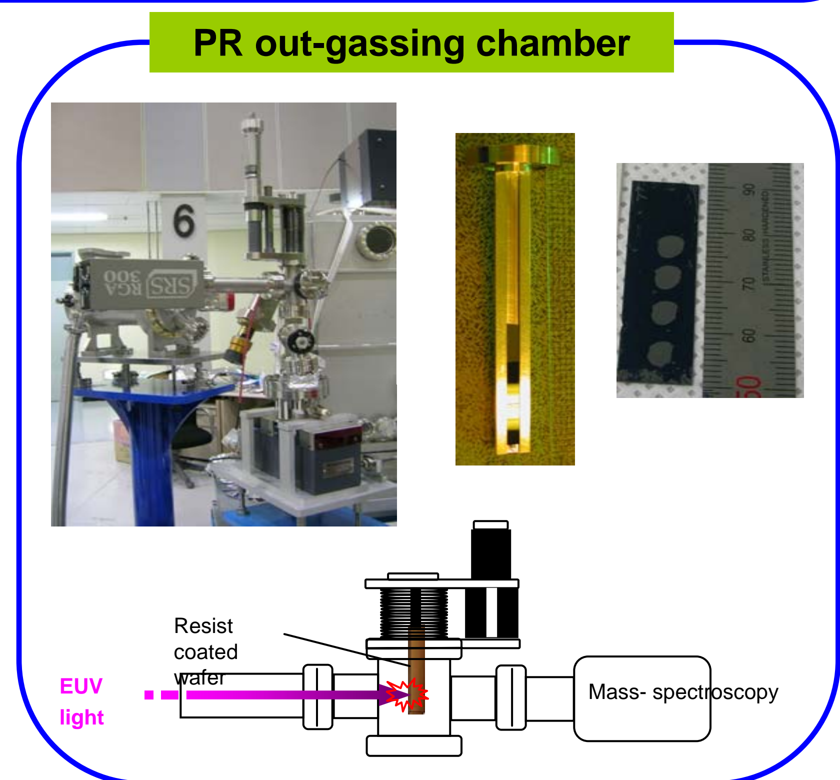
Industry - Samsung Electronics, Dongjin Semichem, IMT



EVUL Beamline at PAL







Thank you

for your attention!