

International EUVI Initiative

**Paolo Gargini,
Vivek Bakshi, Kim Dean, Phil
Seidel, Stefan Wurm**

**October 18th, 2006
Barcelona, Spain**

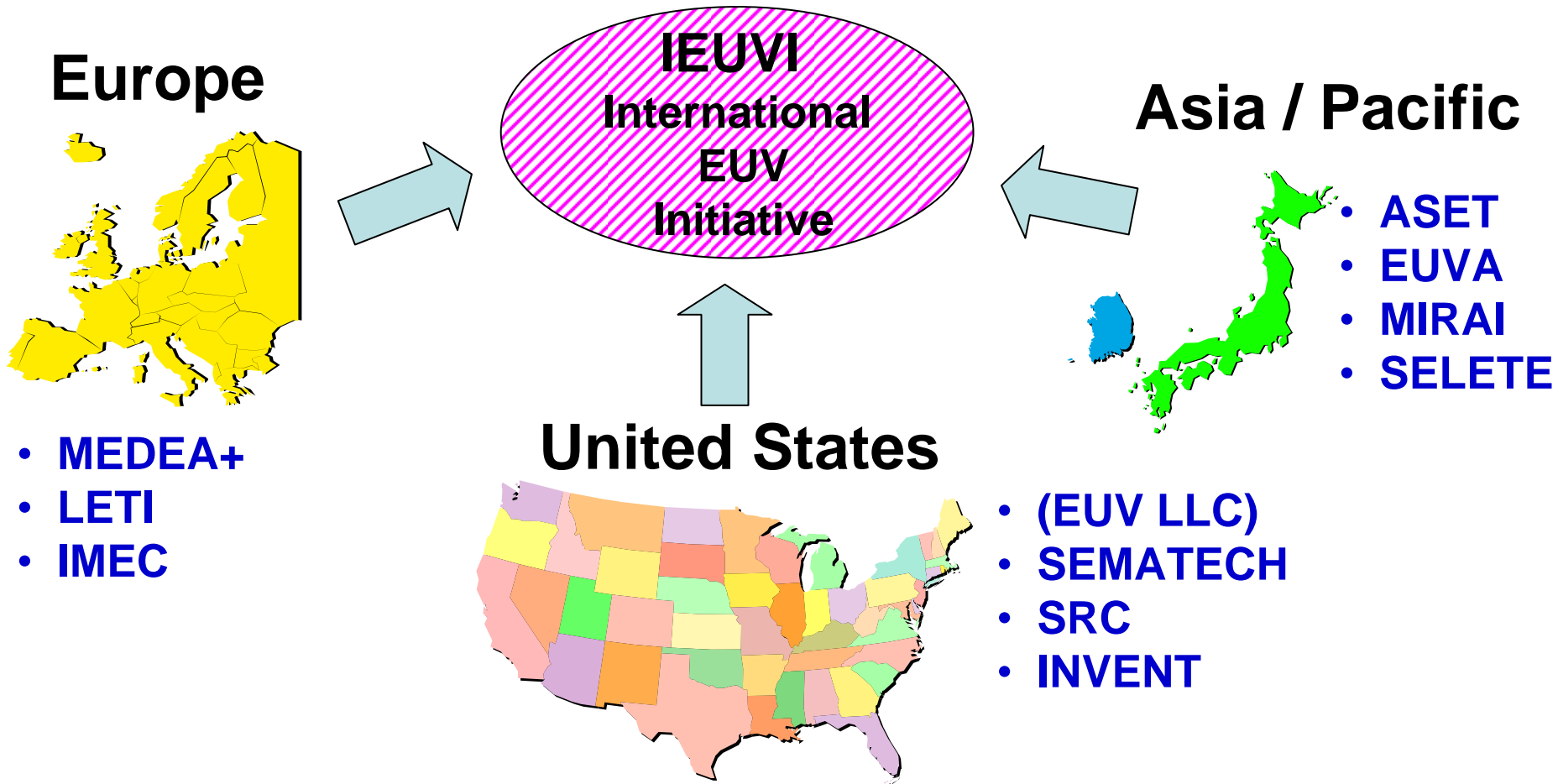


Disclaimer

- **The content of this presentation represents the opinion of the author and it has no relation to the opinion of Intel or of its employees**
- **I like to thank all the IEUVI TWG members that have generously provided data and slides**
- **They will also answer all the questions in great details, so please:**
 - **“Ask freely!”**
 - **Thanks**
 - **Paolo Gargini**

Once upon a time, a
long long time ago.....

International EUV Initiative (IEUVI)...



IEUVI Mission: To further the coordination of collaborative efforts among leading EUVL R&D consortia.



IEUVI – What, How, and Who

- **What:** To address infrastructural issues that need to be resolved for EUVL commercialization.
- **How:** The IEUVI collects technical inputs through its Technical Working Groups (TWGs), and identifies possible show stoppers for commercialization.
- **Who:** IEUVI TWG members include integrated device manufacturers, suppliers, national laboratories and universities.

EUV Commercialization



IEUVI Organization

IEUVI Board

Chair:	Paolo Gargini	ITRS		
Member Organizations:	CEA / LETI	(EU)	ASET/Selete	(JP)
	IMEC	(EU)	EUVA	(JP)
	MEDEA+	(EU)	SEMATECH/Albany	(US)

IEUVI Technical Working Groups (TWG)

Mask TWG

Chair:	Phil Seidel	(US)	SEMATECH
Co-Chairs:	Iwao Nishiyama	(JP)	ASET
	Jinho Ahn	(KR)	Hanyang Univ.
	Jan Hendrik Peters	(EU)	AMTC
	Phil Seidel	(US)	SEMATECH
Meeting			
Organizer:	Shinji Okazaki	(JP)	ASET

Optics Contamination TWG

Chair:	Andrea Wuest	(US)	SEMATECH
Co-Chairs:	Yasuaki Fukuda	(JP)	EUVA / Canon
	Bas Mertens	(EU)	TNO
	Tom Lucatorto	(US)	NIST
Meeting			
Organizer:	Giang Dao	(US)	SEMATECH / Intel

Source TWG

Chair:	Koichi Toyoda	(JP)	EUVA
Co-Chairs:	Stefan Wurm	(US)	SEMATECH / Infineon
Meeting			
Organizer:	Dieter Gotz	(EU)	MEDEA+
	Masashi Ogawa	(JP)	EUVA
Facilitator:	Vivek Bakshi	(US)	SEMATECH

Resist TWG

Chair:	Kim Dean	(US)	SEMATECH
Meeting			
Organizer:	Serge Tedesco	(EU)	CEA / LETI

IEUVI Meetings

- First meeting held on Feb 26th, 2001
- 18 meetings held to date
- Meetings scheduled in conjunction with SPIE, EUV Symposium, etc
- Meeting number 19 scheduled for this Friday, October 20th, 2006

1. Source TWG: Goal & Objective

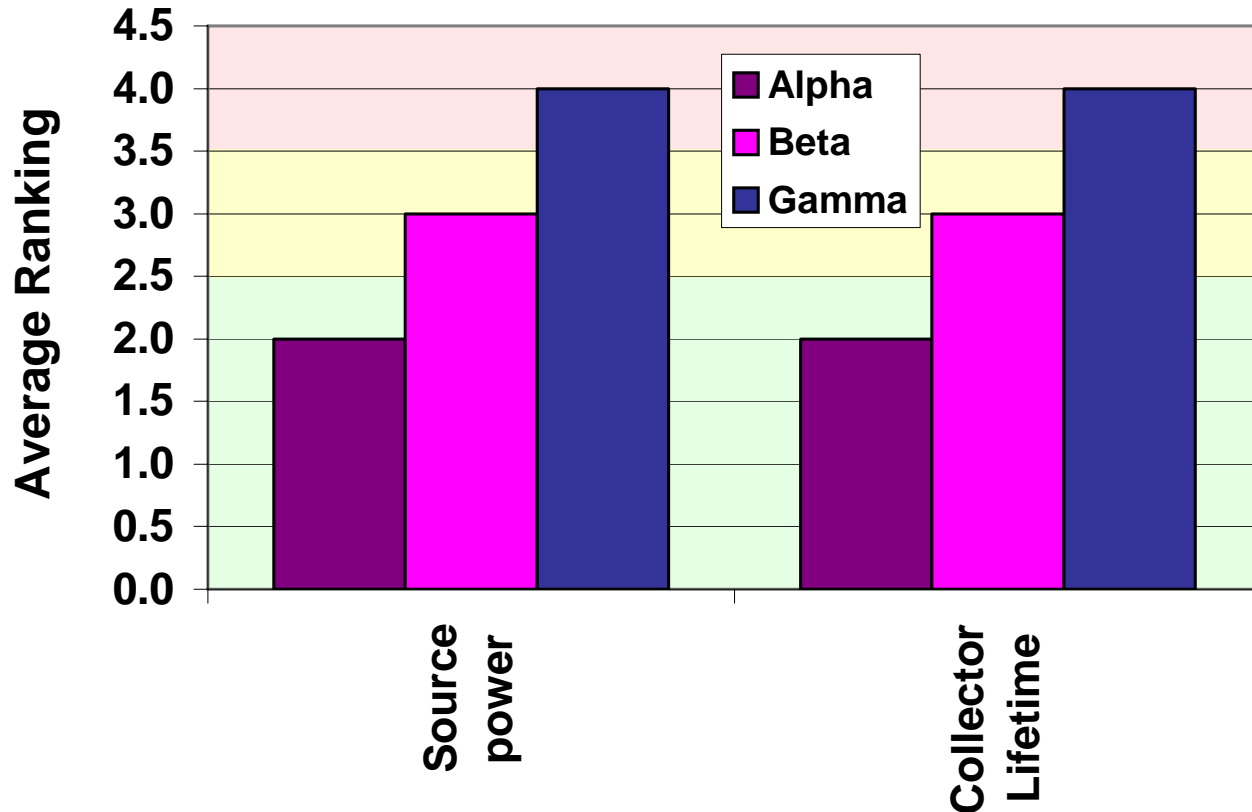
- **Goal:** Provide a platform for all stake-holders
 - Identify EUV critical issues, and develop consensus on critical technical challenges
 - Foster collaborations in metrology & interfaces standardization
- **Objective:** Accelerate consensus building in the industry
 - Coordinate key messages to the broader source community
 - Support source benchmarking efforts (power, out-of-band, debris)

1. Source TWG: Accomplishment

- **Drive standards development**
 - Development of specifications for collector lifetime requirements for alpha, beta and gamma level EUV sources
 - Development of standards for Intermediate Focus (IF) metrology
 - Identified interface opportunities for the industry to reduce cumulative development costs
- **Drive industry consensus on critical technical challenges for EUV source commercialization**
 - Identify and rank critical issue for EUV source technology
 - Map which of the stake holders will be addressing which EUV source critical issue and which issues are not being addressed
 - Need for spectral purity filters

1. Source TWG: Gap Analysis

- 11 responses to Gap Survey for 2 source metrics



- Industry experts see no manufacturable beta tool solution.
- A significant additional effort is required to close this gap

Survey assumed:

Alpha	2006/07
Beta	2009/10
Production	2012/13

Ranking Criteria =

1.0 Manufacturable solutions exist, and are being optimized
 2.0 Manufacturable solutions are known but needing further development

3.0 Interim solutions known

4.0 Manufacturable solutions are NOT known



1. Source TWG: Development Gaps

- Fundamental Understanding
 - Debris generation and control
 - Physics of power scaling (vacuum sparks with rotating electrodes)
 - New source/scanner designs (e.g. field array, high throughput scanners)
- Engineering Development
 - Challenging source/collector integration
 - Improvement of component designs/materials for longer lifetime
 - Designs that can handle heat dissipation
- Interdisciplinary Center of Excellence (CoE)
 - To support the industry with new ideas a CoE is needed
 - Among others the CoE must have core competencies in modeling, materials development, plasma-material interaction, advanced source metrology, and debris mitigation
- R&D Cost for EUV sources is estimated to be 2-2.5 higher than for light sources current lithography technologies

1. Source TWG: Recommendations

- Research & development collaborations can accelerate source readiness
 - Collaborations can provide a much better use and coordination of available resources
 - Collaborations can significantly reduce the time to market for commercial EUV sources
- Focus resources on Sn DPP technology that can deliver beta level EUV sources in 2009
 - Only spend big development-\$ on source that does have a viable path for delivering a beta tool source in 2009 – down select now
 - Abandon the dual technology path for beta type sources and only spend small research-\$ on second generation sources (DPP or LPP)
- The industry needs to commit to a beta tool source soon
 - The industry must combine resources to enable an early test bed for beta tool sources
 - Such a test bed would be best located at a scanner manufacturer or at an industry consortium. The preferred test bed is a beta tool.

2. Optics TWG: Goal & Objective

- **Goal:** Increased cooperation in the EUV optics lifetime/contamination area
 - Understand scaling laws for extrapolating lifetime testing to production requirements
 - Understanding of fundamental processes that determine EUV optics lifetime
- **Objective:** Share testing protocols and procedures to ensure lifetime data as measured by different group is comparable

2. Optics TWG: Accomplishment

- Established the link between lithographers and surface science experts
 - Directly impacts capping layer development work and lifetime testing protocols used to test capping layers
 - Know-how transfer from surface science to exposure tools and optics suppliers and vice versa
- Provided “gold-standard” multilayer samples to the industry
 - Such samples allow to compare lifetime testing between different facilities without having the need to disclose proprietary testing conditions
- Highlighted the difficulty of verifying progress in optics lifetime

2. Optics TWG: Development Gaps

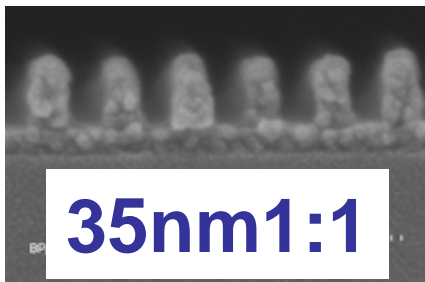
- Fundamental Understanding
 - Fundamental study of the impact of EUV radiation, including frequency, and interactions between EUVL tool environment and capping layer material
- Engineering Development
 - The progress of capping layer development is significantly gated by the availability of standard capping layer life time test technology
 - Benchmarking of capping layers with data feedback and sharing
- Capping layer cleaning strategy
 - Lack of data that demonstrates working cleaning strategies under production tool conditions
 - In-situ metrology may be needed for cleaning strategies to work
- Novel capping layer identification and development
 - There is currently no back-up solution for Ruthenium capping layers
 - R&D on alternative capping layer material is required

2. Optics TWG: Recommendations

- Accelerate fundamental understanding of process limiting capping layer lifetime
 - Collaborations between tool/optics suppliers and surface science institutions to test capping layer under realistic conditions
 - Make testing facilities available for screening of promising new capping layers with no proprietary information exchanged
- Exposure tool manufacturers should share more information about lifetime testing and tool conditions
 - This information is required to assess optics lifetime readiness
- Lifetime testing is complicated and not well-understood
 - The industry must share more data on protocols, testing conditions, metrology etc.
- The industry must develop accelerated lifetime testing to enable optics testing for the required 30,000 hours lifetime

3. Resist TWG: Goal & Objective

- **Goal:** Increased cooperation among EUV resist community world wide
 - Develop resist specification roadmap
 - Coordinate efforts to address top 3 issues
- **Objective:** Share data and information to speed development of EUV resist



≡

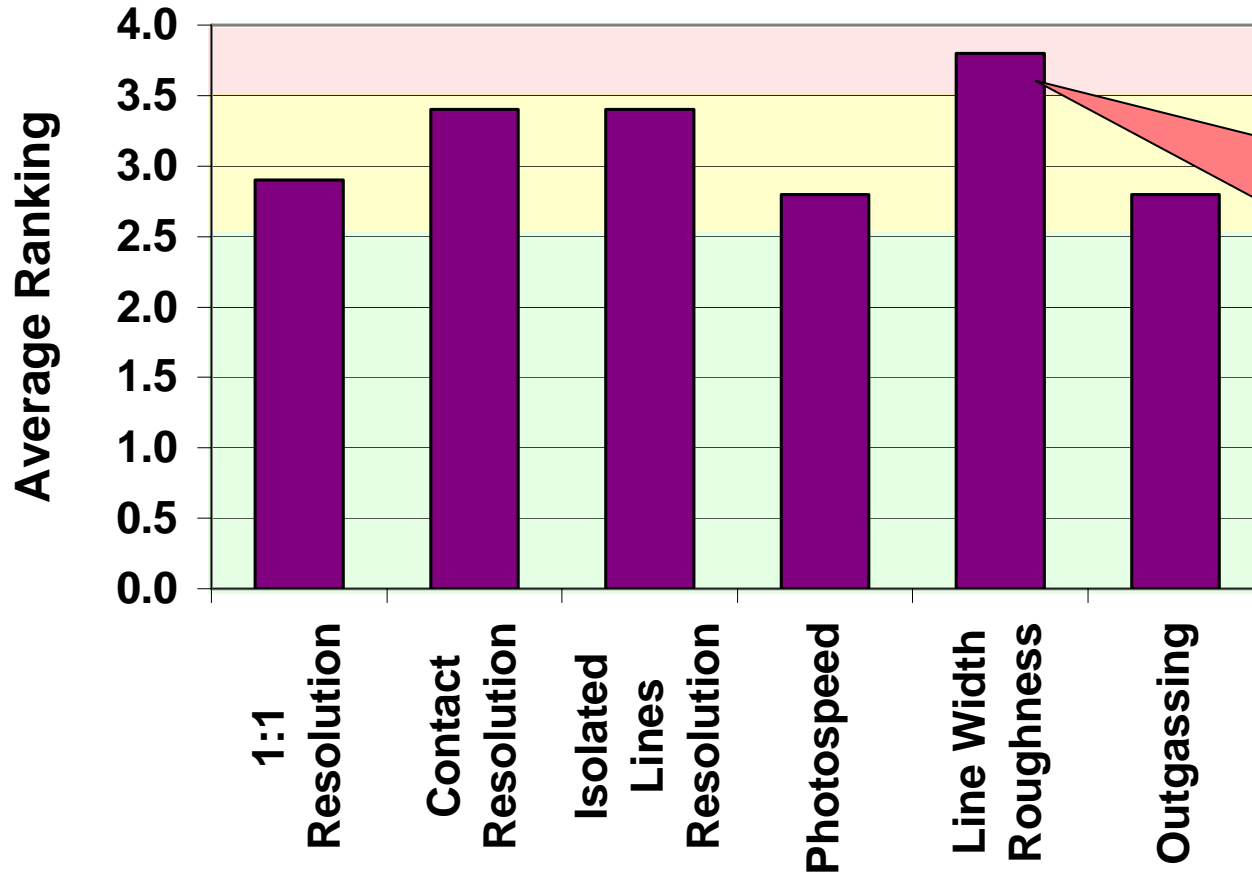
Shared information that helps to coordinate and focus industry resources!

3. Resist TWG: Accomplishment

- Six researchers from Japan, US and Europe participated in the round robin testing
- All participants tested a model resist and reported the results at resist TGW meetings
- The TWG round robin testing revealed the lack of common and/or cross-calibrated methodologies and measurement techniques for outgassing
- => Global collaboration is important to reach consensus on methodology and results

3. Resist TWG: Gap Analysis

- 8 responses to Gap Survey for 6 resist metrics



LWR is the biggest concern. Is it possible to meet all specs simultaneously?

Survey assumed:
 Alpha 2006/07
 Beta 2009/10
 Production 2012/13

Ranking Criteria

IEUVI

- 1.0 Manufacturable solutions exist, and are being optimized
- 2.0 Manufacturable solutions are known but needing further development
- 3.0 Interim solutions known
- 4.0 Manufacturable solutions are NOT known



3. Resist TWG: Technical Gaps

- Contact Resolution
 - There is very little contact hole data available. Based on acid diffusion considerations, resolution will be a big problem.
- Isolated Line Resolution
 - Flare will be a major concern for isolated lines - need flare spec.
 - Resist is not the critical issue given good substrate adhesion.
 - Film thickness may not support "next step" in processing.
- Line Width Roughness (3σ)
 - Fundamental research is required to reduce the LWR.
- Photospeed
 - Ultimately this is linked to EUV source, resist cannot do it alone.
 - Photospeed by itself has been demonstrated and is not an issue.
 - But difficult to simultaneously meet photospeed and LWR specs.
- Outgassing
 - Need clear direction on methodology and specifications.

3. Resist TWG: Recommendation

- Resist vendors need sizeable joint development projects with end customers
 - IC manufacturers need to engage resist suppliers (\$)
- Suppliers need more tool access for 32 nm half pitch resist optimization
 - IC manufacturers and consortia are being asked for MET and Alpha tool exposure time access (\$\$\$)
- Beyond 22nm HP, non-CAR system is necessary
 - Developing new resist platforms takes a very long time and EUV photons to support it are needed in 2007/08
 - To avoid repeat of EUV photon bottleneck seen for 32 nm hp development resist suppliers must have their own in-house, standalone, affordable EUV Interferometric lithography tools. (\$\$)

4. Mask TWG: Goal & Objective

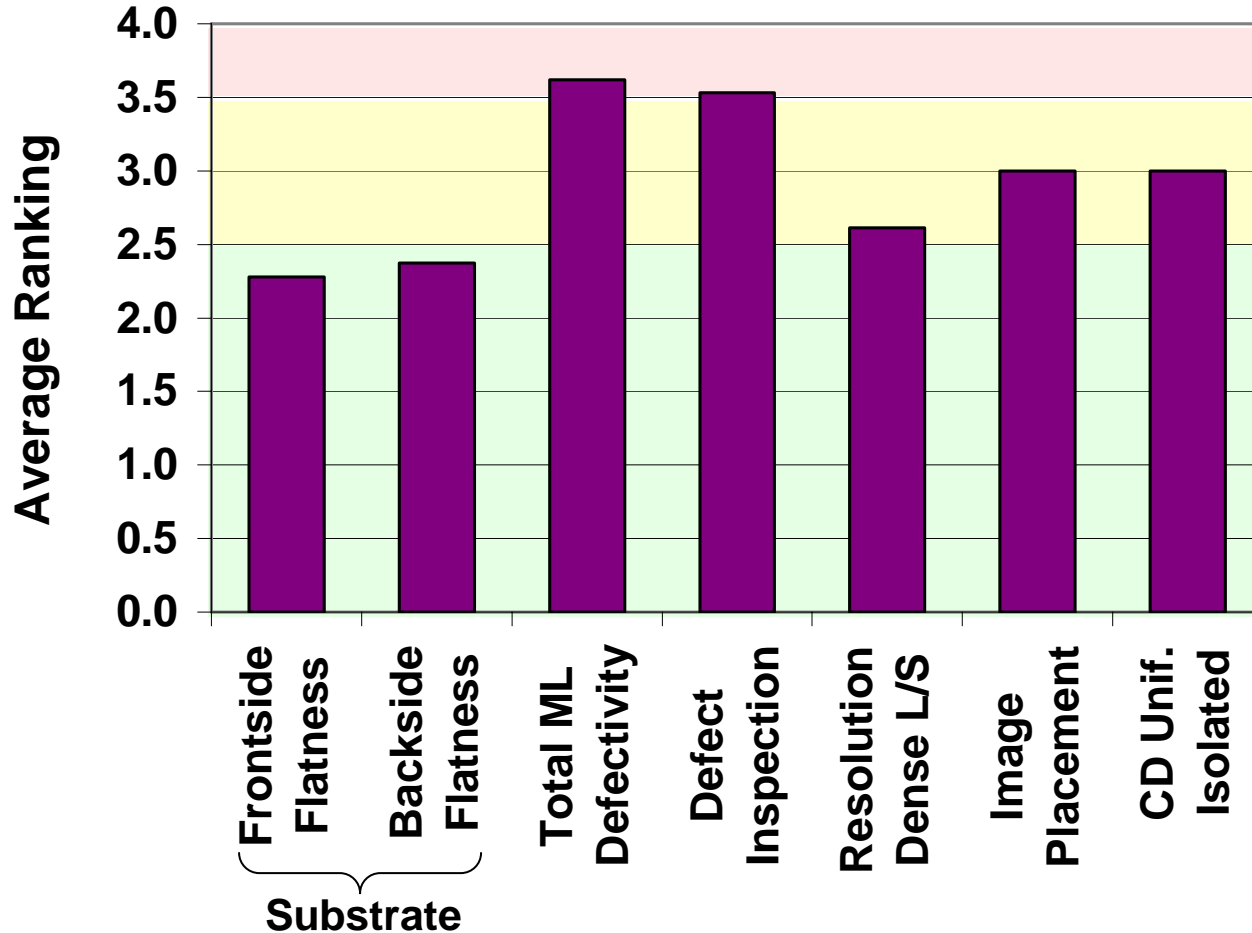
- **Goal:** Provide a forum to support and foster improved EUV Mask Infrastructure Developments
 - Review key regional updates to IEUVI Mask TWG representatives to improve global knowledge base (deter duplication of efforts where possible)
 - Foster collaborative activity in key areas to reach consensus:
 - Commercial EUV Mask requirements
 - EUV mask standardization (especially carriers and handling)
- **Objective:** Develop agreed to critical issues and needed progress versus requirements (roadmaps) to accelerate development
 - Assess continual progress and elevate key issues / showstopper items to correct industry levels
 - Develop resolution plans or required activity to help provide solutions to key issues

4. Mask TWG: Accomplishment

- **Drive industry consensus on current performance versus critical commercial needs and critical technical challenges for EUV mask commercialization**
 - Successfully updated IEUVI Mask TWG “EUV Mask Critical Issues versus Progress” chart w/ consensus input for last 3 yrs (6 cycles)
 - Successfully updated IEUVI Mask TWG “Performance versus Spec. Roadmap” tables w/ consensus input for last 2 yrs (4 cycles)
 - Expanded TWG global participation to include EU, JP, KR, and US
- **Recently completed comprehensive EUV Mask “Gap Analysis” Assessment that included input from 18 organizations that represent IEUVI Mask TWG members**
- **Help drive standards development**
 - Providing additional guidance on the EUV substrate / EUV mask flatness requirements.
 - Providing guidance / direction on the EUV mask carrier & load port standards developments. Review progress versus goal and schedule.

4. Mask TWG: Gap Analysis

- 18 responses to Gap Survey for 7 mask specifications



- Industry experts see total multilayer defects and defect inspection capability as the 2 top risks.
- Pattern placement and CD Uniformity are seen as #3 and #4 critical issues

Survey assumed:
 Alpha 2006/07
 Beta 2009/10
 Production 2012/13

Ranking Criteria



=

1.0 Manufacturable solutions exist, and are being optimized 2.0 Manufacturable solutions are known but needing further development	3.0 Interim solutions known	4.0 Manufacturable solutions are NOT known
---	-----------------------------	--



4. Mask TWG: Development Gaps

Total Multilayer (ML) Defectivity & Defect Inspection

- ML deposition technology, cleaning processes, and inspection capability need additional focus.
- Defect inspection sensitivity down to 25nm size is needed to make progress.
- Total defectivity needs to include patterning stack layers.
- Improvement rate vs. 32nm HP insertion in 2011-2012 is a concern.
- Additional funding from \$15M (per blank supplier) to \$100M (for tool suite = deposition + inspection tool + surface prep / cleans) to achieve ultimate specification.
 - Additional funding of > \$10M required for next generation inspection tool. Consortia should continue development of such tools.
 - Actinic defect inspection may be required for 32nm HP

4. Mask TWG: Development Gaps

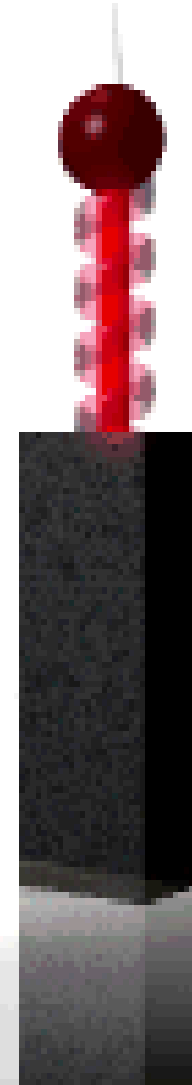
Image Placement (IP) & Critical Dimension Control

- 2 consensus groups for Mask IP issues
 - A: Issue is Not EUV specific and mask industry to focus solely on the limitations of pattern generator, IP metrology, etc.
 - B: Pattern generator & IP metrology improvements needed BUT coupled to substrate & blank flatness control which IS EUV Specific
- E-beam writer
 - \$50M - \$75M gap exist for newer e-beam writer for 32nm HP; writer supplier R&D funding = \$25M (total program is \$75-\$100M) Multi-beam or character projection may be needed.
 - Temperature control for e-beam resists is an issue.
- New IP metrology required for 0.7 nm IP accuracy
 - \$18M gap for new platform versus supplier R&D budget (total program is \$25M - \$35M)
- Some kind of reticle non flatness compensation will be required and further investigation of IP impact is needed
- Mask materials suppliers ability to meet flatness requirements cost effectively

Summary

- The IEUVI has been addressing infrastructural issues that need to be resolved for EUVL commercialization
- The IEUVI TWG's have identified critical issues and are driving resolution through coordinated efforts among its members
- TWG members include IC manufacturers, suppliers, national laboratories, and universities
- The TWG's provide through their members a unique opportunity to interact and to provide inputs to the broader community on relevant issues

Thank you!



Back-up slides



Mask TWG: Survey Results

- Total Multilayer (ML) Defectivity is the highest risk: Rank 3.6
- Defect Inspection Sensitivity: Rank 3.5
- Mask Image Placement (IP) and Critical Dimension (CD) Control were tied: Rank 3.0
- Mask Minimum Primary Image Size: Rank 2.6
- Substrate Flatness: Rank 2.0

1.0 Manufacturable solutions exist, and are being optimized

2.0 Manufacturable solutions are known but needing further development

3.0 Interim solutions known

4.0 Manufacturable solutions are NOT known

Mask TWG: Members

- Alcatel
- AMD
- AMTC
- Asahi Glass Co.
- ASET
- ASML
- Canon
- Corning Inc.
- Dai Nippon Printing
- Hanyang University
- Hoya Corp.
- IBM
- IMEC
- Intel
- Infineon
- Lasertec
- Lawrence Berkeley N.L.
- Nikon
- NuFlare Technology Inc.
- Qimonda
- Samsung
- SELETE
- SEMATECH
- SUNY Albany
- Toppan Printing Co.
- Toshiba
- Veeco Instruments Inc.

IEUVI Mask TWG Top Technical Issues

	<i>Critical Issue</i>	<i>Status</i>	<i>Progress</i>
1	Multilayer defect density (includes substrate)		SIGNIFICANT PROGRESS <i>Limited by inspection</i>
2	Metrology / defect inspection and potential need for actinic inspection for blanks <ul style="list-style-type: none"> • Optical inspection tool path to <30nm PSL • Actinic inspection tool path – commercialization (yellow) 		<i>Limiting further ML defect progress</i>
3	Handling & protection of patterned masks		<i>Data just becoming available; Limited by inspection</i>
4	Patterned mask defect inspection & printability		<i>Recent elevated concern</i>
5	Patterned mask cleaning		
6	Multilayer repair for amplitude defects		<i>Phase repair “not likely”; amplitude unchanged</i>
7	Substrate flatness and thickness variation		PROGRESS, discrepancy on methods
8	IP distortion caused by chucking, included ML stress, and backside Cr layer requirements (adoption)		<i>Continued discrepancy on best methodology</i>

IEUVI Mask TWG Improvement Roadmap: EUV Substrates and Blanks (Feb '06)

Parameter	Current Status	Alpha (2006 - 07)		Beta 32nm HP (2009 - 10)		Gamma '12-13 (32nm HP)	
		Spec.	Comments	Spec.	Comments	Spec.	Comments
Mean CTE (\pm ppb/ $^{\circ}$ K)	10	20	multiple suppliers (Corning, Ohara, etc.)	10	multiple suppliers (Corning, Ohara, etc.)	5	SEMI P37-1102
CTE Spatial Var. (+ ppb/ $^{\circ}$ K TIR)	10	10	multiple suppliers (Corning, Ohara, etc.)	8		6	SEMI P37-1102
Flatness Frontside (nm P-V)	45nm (best) 130nm (routine)	100	Commercial	50	45nm Commercial	32	SEMI P37-1102
Flatness Backside (nm P-V)	70nm (best) 180nm (routine)	100	Commercial	50	70nm Commercial (SEMATECH report)	32	SEMI P37-1102
HSFR (nm rms)	0.10 (best) 0.13 (routine)	0.25	Commercial	0.2	Commercial	0.15	Commercial SEMI P37-1102
Front Surface Local Slope (mrad 3σ)	0.8 (best) 5.0 (routine)	5	Commercial	3	0.8 Commercial (Sematech / LBL report)	1.8	0.8 Commercial (Sematech / LBL report)
Substrate Total Defects @ PSL	14 @ 53nm LTEM (MBDC) 0 @ 43nm FS (MBDC)	50 @ 60nm	Commercial	10 @ 35nm	~0 @ 43nm PSL QZ (MBDC)	0 @ 30nm	SEMI P37-1102 (30nm PSL need)
Total ML D.D. (def./cm 2 @ PSL)	0.025 @ 80nm (MBDC) 0.09 @ 70nm (MBDC) 0.10 @ 80nm (Com.)	0.30	Veeco - SEMA. best [some Commer. cap.]	0.03	0.025 d/cm 2 @ 80nm Veeco at MBDC	0.003	SEMI P38-1103
Cut-off Size (PSL equivalent, nm)	70nm (ML) Lasertec MBDC 54nm (sub) Lasertec MBDC	80	Lasertec M1350	40	Lasertec M7360	25	SEMI P38-1103
Peak Refl. (%)	65.0 (best) 64.0 (routine)	>65.0	Commercial	>66.0	Veeco - SEMA. MBDC	>67.0	SEMI P38-1103
Peak Refl. Unif. (%P-V) Absol.	0.06 (best) 0.40 (routine)	< 0.69	-Veeco - SEMA MBDC -Com. (SEMA report)	< 0.47	-Veeco - SEMA MBDC -Com. (SEMA report)	< 0.33	Commercial SEMI P38-1103
Median Central λ Offset (nm)	0.00 (best) 0.04 (routine)	< +0.09	Commercial (SEMA report)	< <u>+0.06</u>	Commercial (SEMA report)	< <u>+0.06</u>	Commercial SEMI P38-1103
Reflected λ Uniformity (nm P-V)	0.022 (best) 0.058 (routine)	0.08	Commercial (SEMA report)	0.06	Commercial (SEMA report)	0.05	Commercial SEMI P38-1103

IEUVI Mask TWG Improvement Roadmap: EUV Masks and Mask Usage (Feb '06)

Parameter	Current Status	Alpha		Beta (32nm HP beta tool)		Gamma (32nm HP)	
		Spec.	Comments	Spec.	Comments	Spec.	Comments
Nominal Image Size (4X)	150 nm	151nm	160nm NIS [AMTC] 150nm NIS [Intel]	120nm	160nm NIS [AMTC] 150nm NIS [Intel]	85nm	32nm HP (ITRS)
Min Primary Size DLS (4X)	89 nm	106nm	89nm Min size [AMTC]; 100nm [Intel];100nm [DNP]	84nm	89nm Min size [AMTC]; 100nm [Intel];100nm [DNP]	59nm	32nm HP (ITRS)
Image Placement (nm 3s multipoint)	7.7 nm	8.0	7.7nm [AMTC]	4.8		3.4	32nm HP (ITRS)
CD Mean To Target (nm)	3.5 nm	4.6	+ 3.5nm [AMTC]	3.6	+ 3.5nm [AMTC]	2.6	32nm HP (ITRS)
Linearity (nm)	5.0	8.7	5.0nm "iso to dense" linearity [AMTC]	6.8	5.0nm "iso to dense" linearity [AMTC]	4.9	32nm HP (ITRS)
CD Unif. IL MPU (3 σ nm)	4.3 nm	5.0	7.9nm 3s (180nm) [AMTC] 4.3nm 3s (200nm) [DNP]	2.7		1.9	32nm HP (ITRS)
CD Unif. DLS (3 σ nm)	4.1 nm	12.0	4.1nm 3s (180nm) [AMTC] 4.5nm 3s (200nm) [DNP]	6.5	4.1nm 3s (180nm) [AMTC] 4.5nm 3s (200nm) [DNP]	4.6	32nm HP (ITRS)
Absorber LER (3s nm)	TBD	3.2	No mask supplier data	2.5	No mask supplier data	1.8	32nm HP (ITRS)
Reticle outgassing in vacuum H2O (mbar l/s after 10 hr)	1.78 X 10 ⁻⁹	1.0 E-4	preliminary ASML performance	5.0 E-5		1.2 E-5	ASML proposal specs
Reticle outgassing in vacuum CxHy (mbar l/s after 10 hr)	2.35 x 10 ⁻⁹	1.0 E-6	preliminary ASML performance	5.0 E-6		1.2 E-7	ASML proposal specs
Reticle outgassing in shipping H2O (mbar l/s after 10 hr)	1.78 X 10 ⁻⁹	1.0 E-4	preliminary ASML performance	5.0 E-5		1.2 E-5	ASML proposal specs
Reticle outgassing in shipping CxHy (mbar l/s after 10 hr)	2.35 x 10 ⁻⁹	1.0 E-6	preliminary ASML performance	5.0 E-6		1.2 E-7	ASML proposal specs
Added Particle per # handling events (@ PSL)	0 / 70 cycles 50nm	<1 / 100 @ 60nm	0 / 70 cycles 50nm [ASML]	<1 / 250 @ 45nm		< ? per 500 @ 30nm	industry target spec needed
Added Particle per # shipping events (@ PSL)	6 @ 50nm	<2 / 100 @ 60nm	6 @ 50nm [SEMATECH - MBDC]	<2 / 100 @ 45nm		< ? per 500 @ 30nm	industry target spec needed

Resist TWG: Members

- AIXUV
- AMD
- ASML
- ASET
- BOC Edwards
- Canon
- CEA/LETI
- Dongjin
- Energetiq
- Fujifilm
- IBM
- IMEC
- Intel
- JSR
- Nikon
- Osaka University
- Philips
- Qimonda
- Samsung
- SELETE
- SEMATECH
- Shin-Etsu
- Sumika/Sumitomo
- SUNY Albany
- Texas Instruments
- TOK
- University of Hyogo

IEUVI Resist TWG Specification Roadmap

Specifications	Alpha (2006-07)		Beta (2009-10)		Production (2012-13)	
	Spec	Current**	Spec	Comment	Spec	Comment
Resolution 1:1	45nm	35nm/45nm (C/S)	32nm		32nm	
Resolution contacts	55nm	TBD	40nm		35nm	
Resolution Isolated Lines	32nm	30nm/40nm (C/S)	25nm		21nm	
Depth of Focus	200nm	100nm for 35-nm 1:1 200nm for 50-nm 1:1	225nm	Dense and isolated; DOF at 10% exposure latitude	225nm	Dense and isolated; DOF at 10% exposure latitude
Photospeed (mJ/cm ²)	10 mJ/cm ²	21mJ/cm ² E-size @ 50-nm 1:1	10mJ/cm ²	Assuming ~30 wph	10mJ/cm ²	Assuming > 100 wph if 5 mJ/cm ² , 115W intermediate focus
Line Edge Roughness (3σ)	< 4 nm	~4 nm @ 50-nm 1:1 ~7 nm @ 35-nm 1:1	< 2.5nm		< 1.7 nm	LWR < 8% etched gate length; gate length = 18 nm
Wall Profile Angle	>85°	80° @ 50-nm 1:1	> 85°	Measure cross-sections	> 85°	Measure cross-sections
Outgassing	4.7E13 molecules/cm ² -sec	1.60E+13	TBD		TBD	
Pattern Collapse	>3	None observed	>3	Aspect ratio 3:1 for all structures	>3	Aspect ratio 3:1 for all structures
Unexposed Film Thickness Loss	< 10%	10nm	< 5%		< 5%	
PEB Sensitivity	< 2.5 nm/deg C	TBD	<1.5 nm/deg C		< 1 nm/deg C	
Delay Stability @ < 1ppb amine	30min	TBD	30 min	a) pre-exposure, b) under vacuum, c) post-exposure	30 min	a) pre-exposure, b) under vacuum, c) post-exposure
Etch Resistance	Similar to novolak	TBD	Similar to novolak		Similar to novolak	

Source TWG: Members

- AMD
- ASML
- Canon
- Carl Zeiss
- Cymer
- EUVA
- Intel
- MEDEA+
- Media Lario
- Nikon
- Philips Extreme
- Xtreme technologies
- PLEX LLC
- Qimonda
- SEMATECH
- Samsung

IEUVI Resist TWG Specification Roadmap

Metric	Unit	Current (DPP)		Alpha ('06-07)	Beta ('09-10)	Production ('12-13)	Next Generation	
		Xe	Sn					
Scanner Delivery	Date			2006	2007	2009	2011	2013
Potential Source Technology	NA	DPP	DPP	DPP	DPP	DPP	DPP/LPP	LPP/DPP ⁽¹⁾
Target Material	NA	Xe	Sn	Xe / Sn	Sn / Xe	Sn	Sn	Sn
Wavelength	[nm]	13.5	13.5	13.5	13.5	13.5	13.5	13.5
Throughput	[wph]					100	100	100
EUV Power @ IF	[W]	<10	<10	10	30	115 ⁽²⁾	>150 ⁽³⁾	>180 ⁽³⁾
Repetition Frequency	[kHz]	2-5	2-5	2	5	7-10	10	> 10
Integrated Energy Stability	[%]	2-5	2-5	5	1	0.3	0.3	0.1
Source Cleanliness	[hours]					>30,000	>30,000	>30,000
Collector Lifetime	10 ⁹ Pulses	1-10 B	1-10 B	1	10	80	> 80	> 80
	[month]			1	3	12	12	12
Electrode Lifetime	10 ⁹ Pulses	10 B	>10 B	1	10	80	> 80	> 80
	[month]			1	3	12	12	12
Projection Optics Lifetime	[hours]					30,000	30,000	30,000
First Illuminator Mirror Lifetime	[hours]			TBD	TBD	TBD	TBD	TBD
Etendue of Source Output	[mm ² -sr]			TBD	TBD	< 3.3	< 3.3	< 3.3
Max. Angle to Illuminator	[sr]			TBD	TBD	0.03-0.2	0.03-0.2	0.03-0.2
Spectral Purity (130-400 nm)	[%]	10-12		TBD	TBD	3-7	3-7	3-7
Spectral Purity (>400 nm)	[%]	2-6		TBD	TBD	TBD	TBD	TBD
Spectral Purity (20-130 nm)	[%]			TBD	TBD	TBD	TBD	TBD

(1) Multiplexed DPP

(2) Assumes resist with 5 mJ/cm² sensitivity

(3) Assumes resist with > 5 mJ/cm² sensitivity

(4) Light-on-hours

IEUVI

 Very high risk

 Significant risk

 Solution exists



Optics TWG: Members

- AMD
- ASML
- ASET
- BOC Edwards
- Canon
- CEA/LETI
- EUVA
- FOM
- Fraunhofer IOF
- Freescale
- Intel
- LLNL
- Nikon
- NIST
- PTB
- Qimonda
- SEMATECH
- TNO
- University of Albany
- University of Hyogo
- University of Illinois
- Carl Zeiss