

22nm Nanoimprint at SEMATECH

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Introduction

SEMATECH has begun development on a 22nm nanoimprint process using Step and Flash Imprint Lithography (SFIL). The work is aimed at assessing SFIL for semiconductor device high volume manufacturing, as well as providing access to high resolution structures for unit process development, tool characterization, and alternative applications. SFIL's exceptional resolution capability and consistent image quality make it the ideal choice for a wide range of development activities ranging from etch development, to metrology and inspection tool characterization, to non-semiconductor uses such as energy and biological applications.

Full 300mm wafer, 22nm SFIL process results including critical dimension uniformity and line width roughness are shown for the first time. The template contains a variety of features such as gratings, gate structures, programmed defects, zone plates, and more.

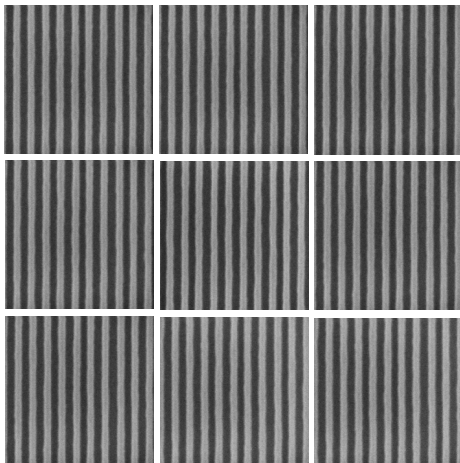
The development results shown here are based on a collaboratively designed, commercially manufactured, template containing non-proprietary structures such that it is accessible by both internal and external customers. By providing public access to an early 22nm imprint process, SEMATECH is helping to further develop SFIL and ensuring its viability as an enabling technology for future applications.

22nm SFIL Assessment

		"Production Grade" Current Status	Flash 2009 ITRS Requirement	Factor Away	MPU 2009 ITRS Requirement	Factor Away	DRAM 2009 ITRS Requirement	Factor Away
Process			2013		2014		2016	
Process	1/2 Pitch	<< Requirement	23nm		24nm		23nm	
	Gate in Resist	<< Requirement	25nm		25nm		25nm	
	Contact in Resist	<< Requirement	32nm		29nm		25nm	
	CDU (3σ)	2.5nm	2.3nm*	1.1x	1.9nm**		2.3nm*	
	LWR	2.5nm	2.3nm	1.1x	1.9nm**	1.3x	2.3nm	1.1x
	Overlay (3σ)	14nm	7.4nm	1.9x	6.0nm	2.3x	4.5nm	3.1x
	Defect Density***	100/cm ²	0.01/cm ²	10000x	0.01/cm ²	10000x	0.01/cm ²	10000x
	Aspect Ratio	2:1 Max	2:1 to 3.5:1	<1.7x	2:1 to 3.5:1	<1.7x	2:1 to 3.5:1	<1.7x
	Templates							
Templates	1/2 Pitch	32nm	23nm	1.4x	24nm	1.3x	23nm	1.4x
	Gate	32nm	25nm		25nm	1.3x		
	Contact	32nm	32nm		29nm	1.1x	25nm	1.3x
	LWR	2.5nm****	2.3nm	1.1x	1.9nm**	1.3x	2.3nm	1.1x
	CDU: Isolated Lines (3σ)				1.9nm**			
	CDU: Dense lines (3σ)	1.75nm****	2.3nm		2.4nm		2.3nm	
	CDU: Contacts/Vias (3σ)		3.2nm		2.9nm		2.5nm	
	CD Mean-to-Target		0.5nm		0.5nm		0.5nm	
	Image Placement (Residual)	2.8nm	4.3nm		3.5nm		2.6nm	1.1x
	Max X,Y Defect Size	>> Requirement	2.3nm		2.4nm		2.3nm	
	Max Z Defect Size	>> Requirement	4.6nm		4.8nm		4.6nm	
Defect Density*****	>> Requirement	0		0		0		
		Meets requirement	<4x away from target					
		<2x away from target	No foreseeable solution in the near future					

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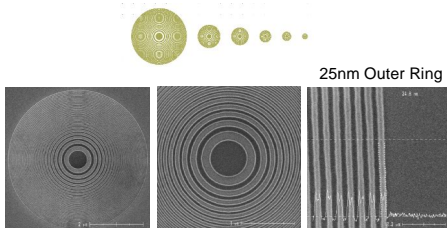
22nm Half-Pitch Performance



- CD
- Average: 19.4nm
- 3 Sigma: 1.0nm
- LWR
- Average: 2.5nm
- 3 Sigma: 0.6nm

(Across wafer results. One site measured per field)

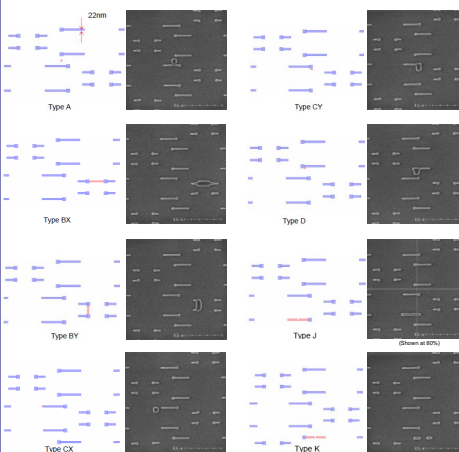
Fresnel Zone Plates



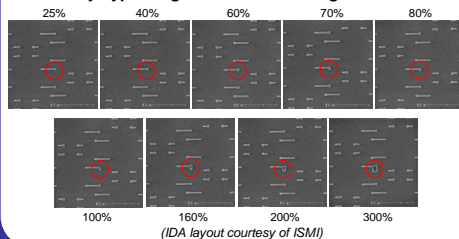
22nm Intentional Defect Array (IDA)

Defect Type	Defect Size (% of Feature Size)									
	25	40	60	70	80	100	160	200	300	
A	x	x	x	x	x	x	x	x	x	
Bx	x	x	x	x	x	x	x	x	x	
By	x	x	x	x	x	x	x	x	x	
Cx	x	x	x	x	x	x	x	x	x	
Cy	x	x	x	x	x	x	x	x	x	
D	x	x	x	x	x	x	x	x	x	
J	x	x	x	x	x	x	x	x	x	
K	x	x	x	x	x	x	x	x	x	

✓ Resolved (Visible on Wafer), ✗ Not Resolved

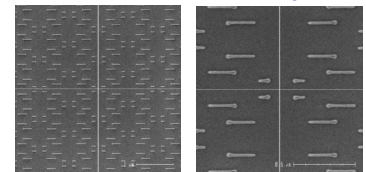


Cy Type Programmed Defect Progression



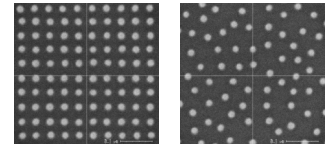
(IDA layout courtesy of ISMI)

22nm SRAM Gate Layer

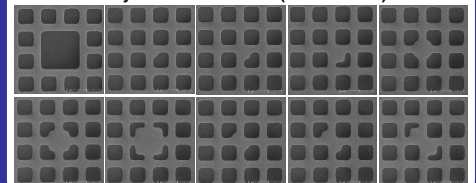


Misc. Features

22nm Dots/Spaces (Grid and Random)



Dummy Fill Macro Defects (~0.3 – 3.0um)



Summary

- A 22nm SFIL process has been established at SEMATECH on a Molecular Imprints Imprio 300.
- A Gaussian beam written template with a minimum feature size of 22nm is available for both internal and external customer use.
- This process and template will be used to support process development, metrology tool characterization, and alternative programs.
- A second template with additional feature sizes and types will be available in late 2010.

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