Integration of EUV-Thickness Resist Processes into MPU Manufacturing Flows

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Integration Challenges

- Defect control
  - Spin-coating ~1000 Å resist films over topography
  - Hardmask deposition and removal
- Hardmask integrations
  - Appropriate etch selectivities
  - Deposition temperatures, surface roughness, removal
  - Chemically inert
- Maintain CD control with topography

Approach

- Build working SRAMs with ultrathin resist (UTR, 1000-1500 Å) processes at gate (line), contact (hole), and metal (oxide trench for copper) levels
- Since current EUV resist strategy focuses on DUV materials, use DUV lithography for integration demonstration with meaningful EUV resists
- Initial demonstration with poly gates and oxide dielectrics, expand into new gate stack and low-k dielectrics

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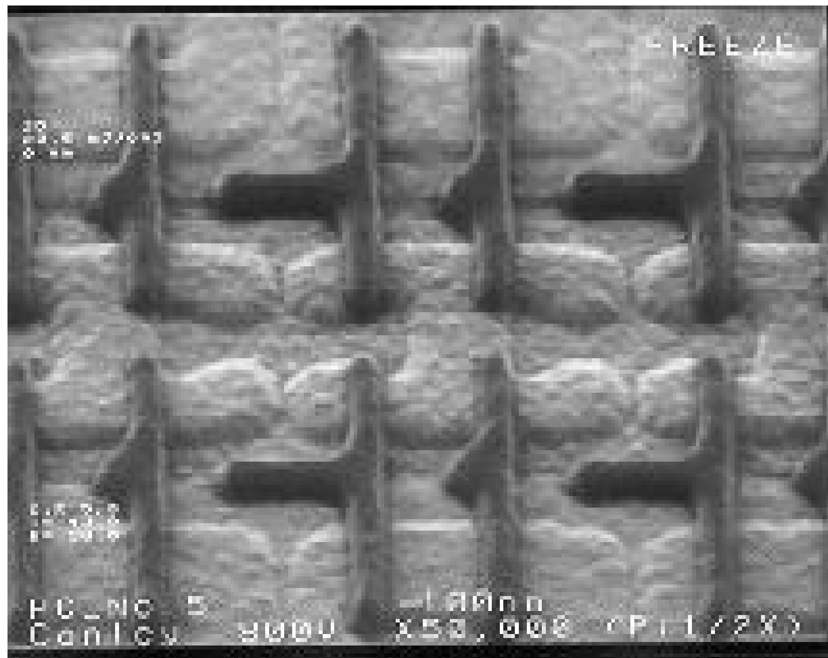
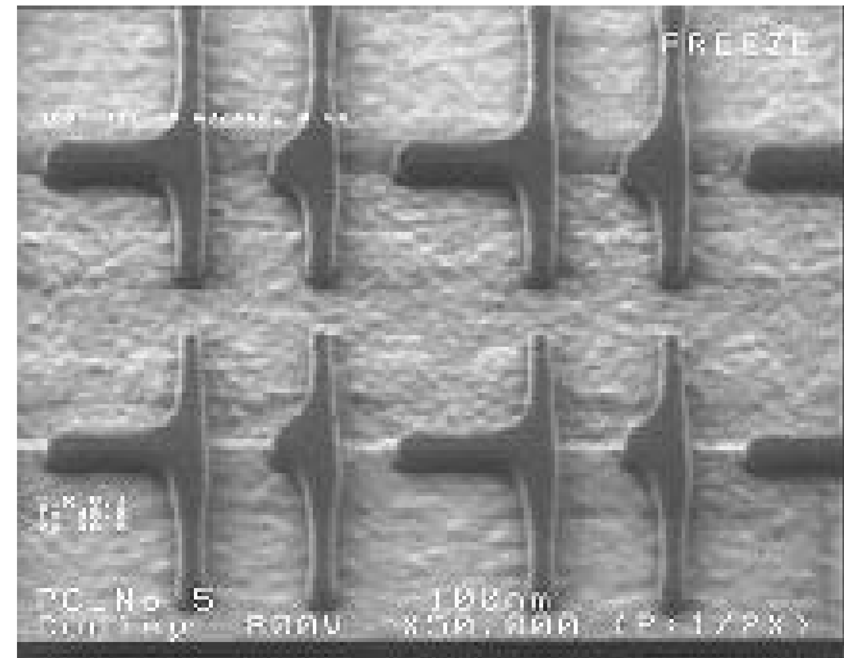
No Issues with 1200 Å Resist Coatings Over Topography

EUV Baseline Resist



Resist A Process



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PSM DUV UTR Line/Space Bossung Data After Develop

Gate Lines

CD (um)

0.2
0.19
0.18
0.17
0.16
0.15
0.14
0.13
0.12
0.11
0.1

-0.6 -0.4 -0.2 0 0.2

Focus (um)

- 18 mJ/cm2
- 19 mJ/cm2
- 20 mJ/cm2
- 21 mJ/cm2
- 22 mJ/cm2
- 23 mJ/cm2
- 24 mJ/cm2

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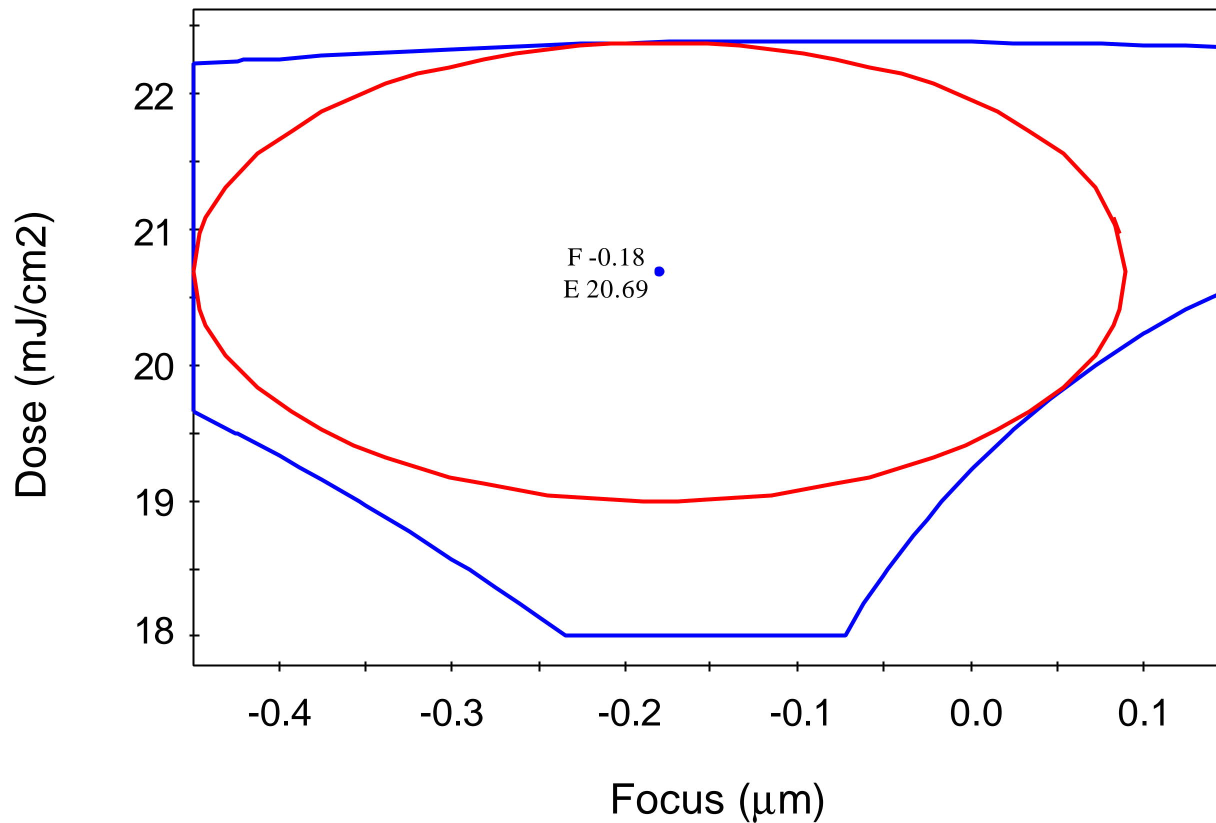
PSM DUV UTR Line/Space Process Window After Develop

DOF= 0.54µm at 16.5% Exposure Latitude



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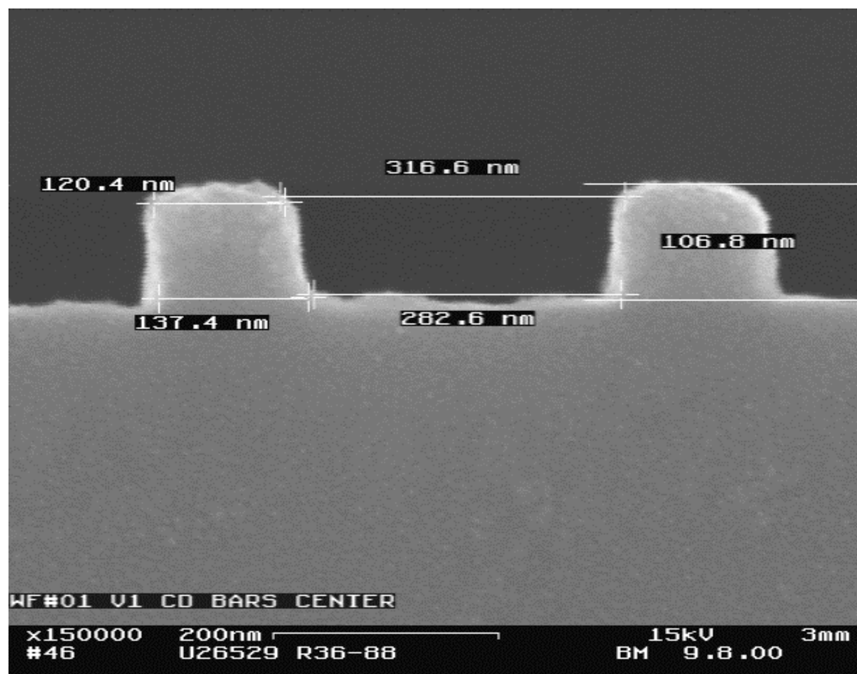
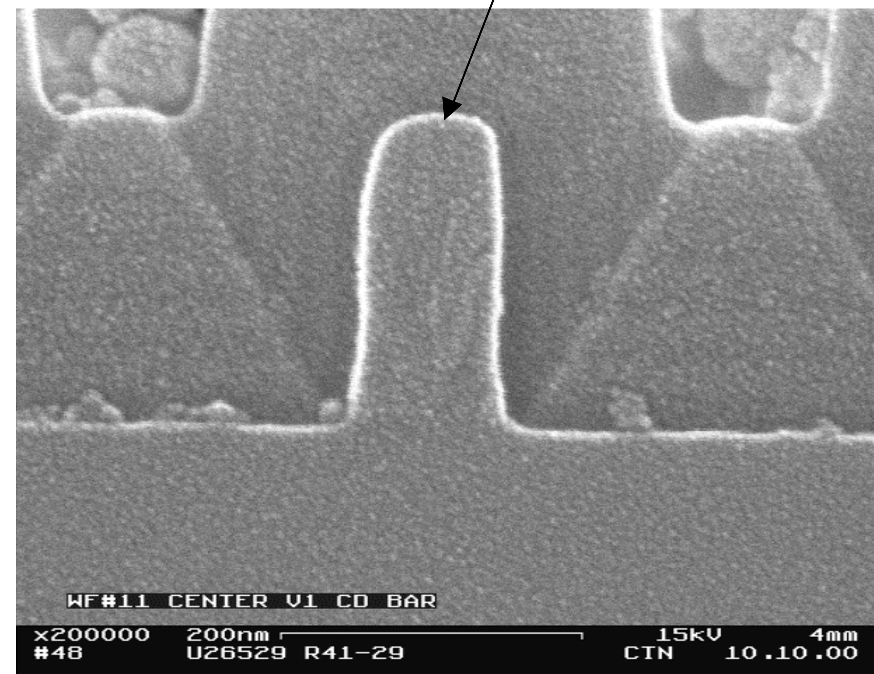
Cross-Sections of 1400 Å Resist Polysilicon Process

Initial Resist Profile

Poly Line After Etch





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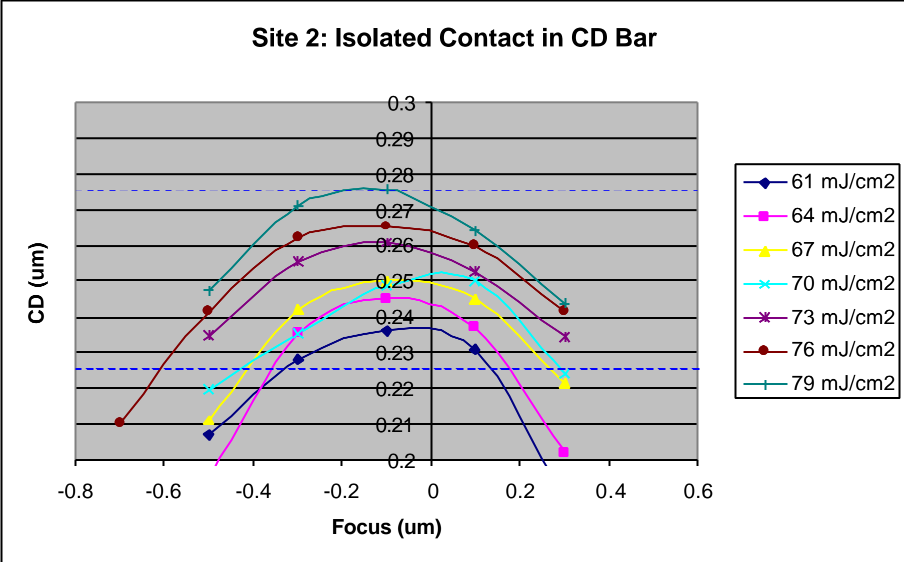
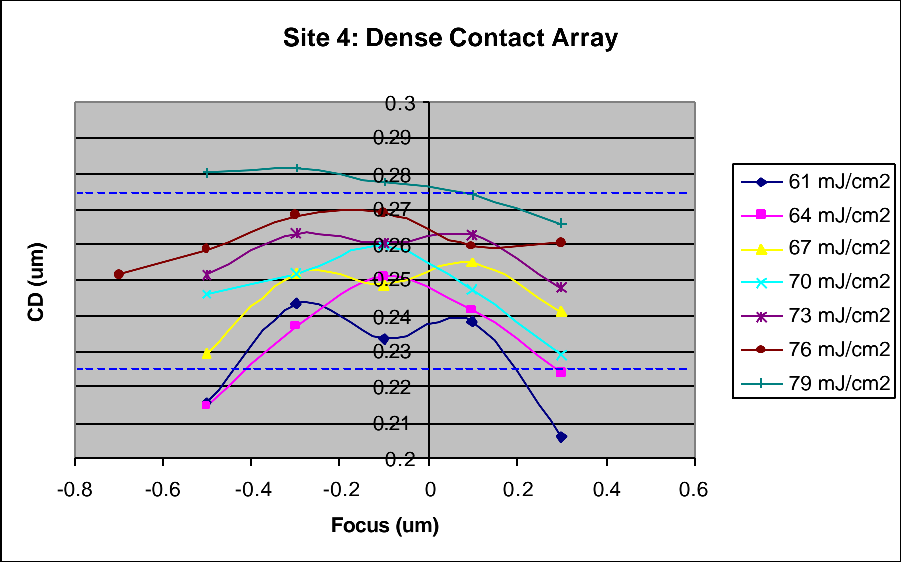
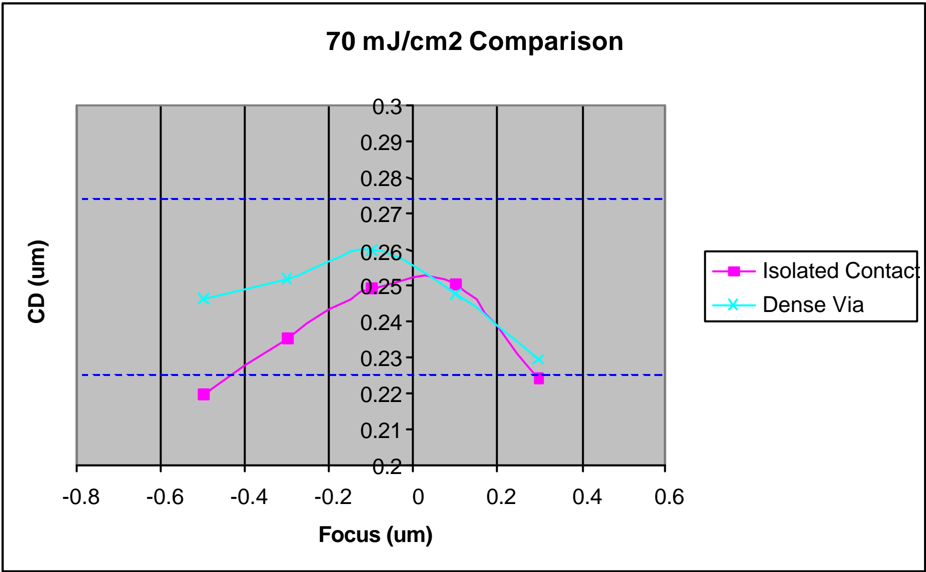
0.25 mm UTR Contact Process After Develop







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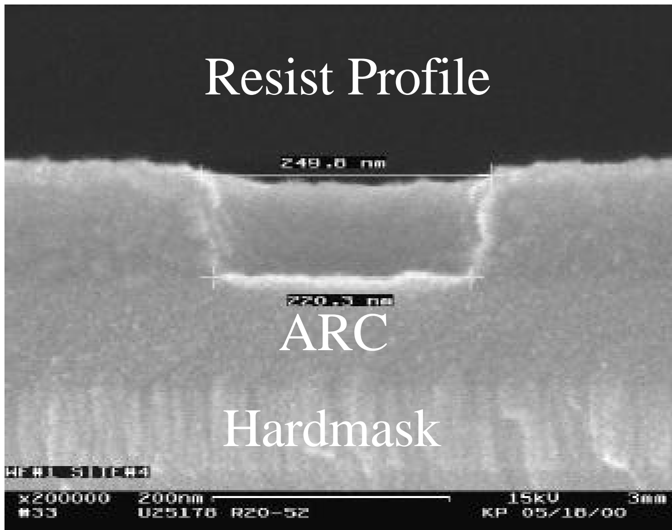
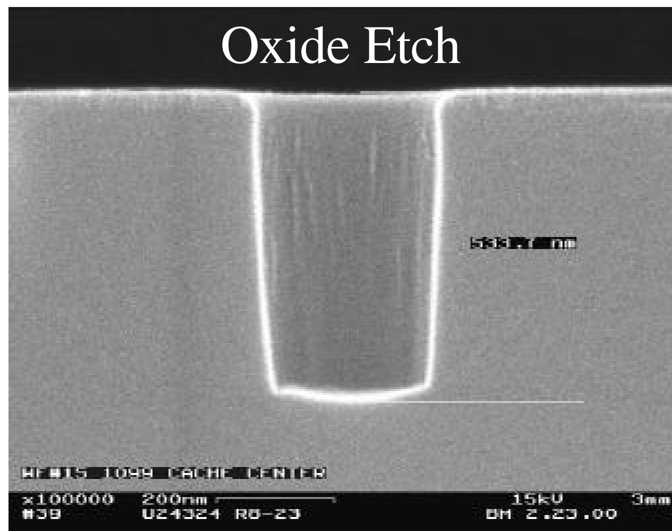
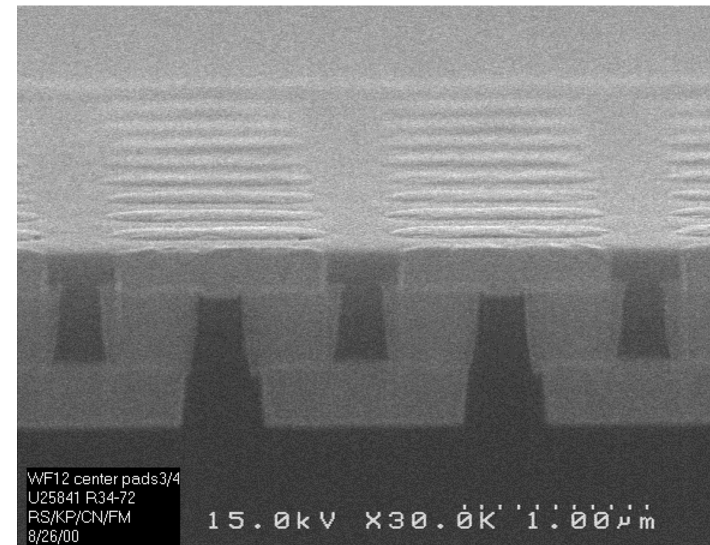
Demonstrated UTR Cu Damascene Integration





Cu damascene Metal 1 to Metal 2 build w/ UTR processes at Via 1 and Metal 2:

- CD control needs improvement



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Chain Yield Data from UTR Cu Damascene Integration

Cumulative Percent

100
80
60
40
20
0

Control Wafers
UTR at Via 1
UTR at Metal 2
UTR at Via 1 and Metal 2

0.0
0.5
1.0
1.5

Contact Resistance (Ω/Via)

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No Issues in Coating Uniformity

Mean
% Std Dev

First boat of 25

Second boat of 25

Thickness in Angstroms

1213.5
1208.5
1203.5
1198.5
1193.5
1188.5

% Std Dev of film unif.

0.29
0.24
0.19
0.14
0.09
0.04

1 5 9 13 17 21 25 29 33 37 41 45 49

Wafer #

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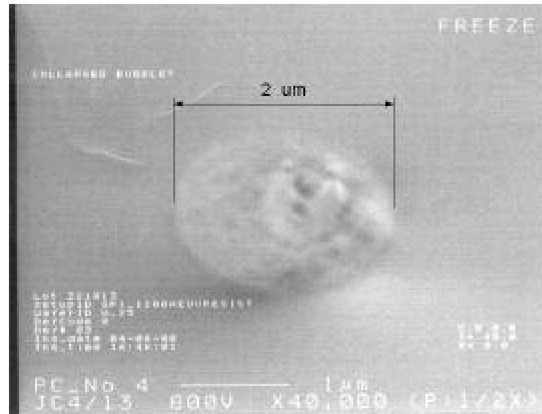
UTR Unpatterned Wafer Inspection and Review

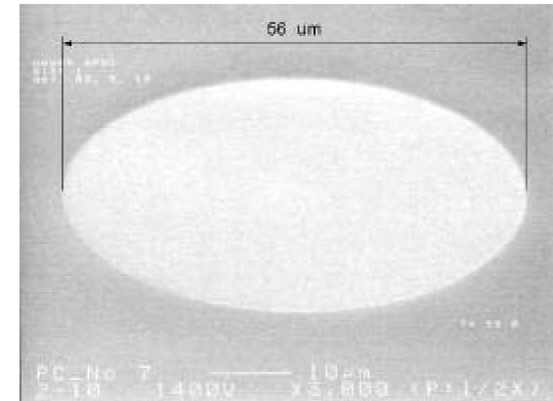
- Defects randomly distributed
- Particles (0.1-0.3 µm) are most prevalent defect

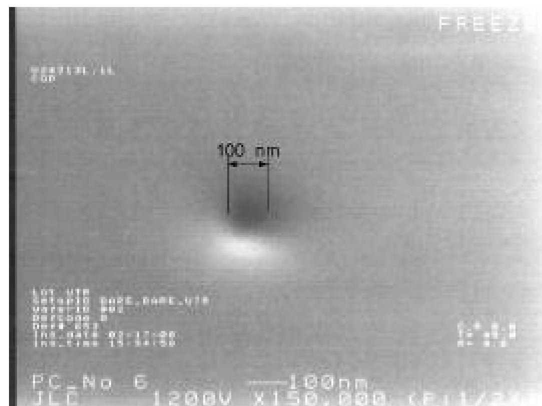
Major Defect Types

Collapsed Bubble



Dewetting Spot





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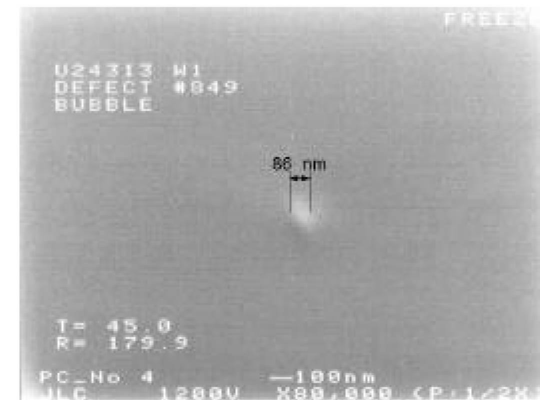

Small Particle

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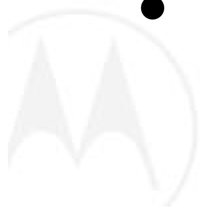
Summary

- Goal: build working SRAM with 1000-1500 Å resist processes at gate, contact, and first metal lines
- No issues seen with gate-level topography before or after etch
- Demonstrated via chain yield in UTR Cu damascene process
- Need to improve CD control
- Small particles, rather than pinholes, most prevalent defect after coating and development
- Full device build lots in progress



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