ISMT / EUV-LLC EUV Mask Development Seminar Meeting

(03/04/02 Westin Santa Clara CA)

Meeting Minutes (P. Seidel)

ATTENDANCE: 72 official signed in registrants

MEETING CHAIRS:

Chuck Gwyn	Intel / EUV-LLC	Principal Meeting Chair
Phil Seidel	International Sematech	Meeting Facilitator (Co – Chair)

PURPOSE:
This meeting was organized to promote the needed industry interest for EUV mask and EUV mask related infrastructure. Presenters outlined the processes required, results of activity done to date, and the needed developments.

EXPECTED RESULTS:
The meeting participants are to understand and provide input to the critical issues facing EUV masks and related infrastructure. There will be discussions to highlight the EUV mask related critical issues and develop possible follow on activities.

MEETING EXECUTIVE SUMMARY:
A total of nine presenters from six different organizations reviewed their progress on EUV substrates, mask blanks, and patterned masks. Commercial suppliers are making progress on reducing mask substrate flatness, roughness and defects. Progress has been made on reducing mask blank defects toward target values for EUVL in high volume manufacturing and defect free blanks are not required if successful implementation of mitigation strategies can be realized. These mitigation strategies including repair of mask blank defects (via e-beam, ion milling, and others) and will enable cost reductions while defect learning continues. Cr and TaN are leading absorber choices with TaN performing better than Cr for mean CD control and inspection. Several companies and commercial mask suppliers have patterned square format EUV masks with sub 100nm node resolution (some even showing initial 45nm node capability). Both mask blank and patterned mask defect inspection and defect reduction tooling requires further developments to meet the unique requirements of EUV and remain the greatest challenge for EUV mask fabrication.

Meeting Agenda:

	Topic	Presenter
1.	Introduction	Chuck Gwyn (Intel / EUV-LLC)
2.	LTEM Substrates (polishing & metrology)	John Taylor (LLNL)
3.	Blank Multilayer Depositions (inspection, repair)	Don Sweeney (LLNL)
4.	Mask Patterning Process	Pei-Yang Yan (Intel)
5.	Mask Inspection & defect Mitigation	Alan Stivers (Intel)
6.	Mask Supporting Infrastructure	Barry Lieberman (Intel)
7.	Infineon EUV Mask Fabrication	Frank – Michael Kamm (Infineon)
8.	Photronics / MCoC EUV Mask Patterning	Dave Walker (Photronics)
9.	EUV Mask Cost of Ownership	Scott Hector (Motorola)
10.	Summary / Risks / Commercialization	Chuck Gwyn (Intel / EUV-LLC)

HIGHLIGHTS OF INDIVIDUAL SPEAKERS

1) Chuck Gwyn (Intel / EUV-LLC) – Principal Chair; Welcome / Overview

Chuck reviewed the current imaging results from the ALS (static images) using reflective masks that demonstrate 70nm dense L/S & 70nm contacts (partial coherence σ= 0.8) and resolution down to 50nm dense L/S using dipole illumination. The outline of the many mask process steps required were shown taking in “raw” LTEM stock material all the way down to the final mask product of repair and storage needs. There are four major areas of activity needed in EUV mask mfg. that can be broken down into the

substrate materials, substrate fabrication / finishing, multilayer and absorber stack deposition, and finally absorber patterning. There is at least two known companies and as many as five in each discipline area today. Chuck reviewed all four of the current SEMI standard activities that cover the need for a EUVL mask (P37-mask substrate, ML & absorber stack SEMI draft 3414, reticle chucking, and storage / handling). Chuck also reviewed the details found in the recent SEMI adopted P37 substrate that calls out flatness, roughness, defectivity, and Coefficient of Thermal Expansion (CTE).

2) John Taylor (LLNL / EUV-LLC) – LTEM Substrates Polishing & Metrology

John reviewed the status of the EUVL mask substrates having the main goal to ensure timely commercial mask substrates for EUV production introduction. An outline of the substrate specific requirements (as specified in SEMI P37) was shown for the 6"x6"x0.25" square format that includes meeting 50nm peak-valley flatness, 0.15nm rms roughness, and 0 defects within the quality area. Also CTE levels of better than 30 ppb/^{o}K are needed. Two current bulk materials are being studied by three commercial substrate suppliers for finishing being Corning ULE^{TM} and Schott Zerodur^{TM}. Best finishing roughness to date are in the range of 0.15nm to 0.30nm rms for these materials. John showed the impact of Ion Beam deposition on the surface roughness. Roughness improvements demonstrations can be improved about 2x. John showed the best results to date on the flatness, roughness, and defectivity from the three suppliers who participate in the ISMT / EUV-LLC substrate benchmarking project (LITH111). Best performances to date are ~0.15nm rms roughness, 250nm P-V flatness, and 0.05 def/cm2 defectivity. Meeting all of these specifications simultaneously will be challenging. John highlighted the development needs for capable metrology for both flatness and defect detection to support the P37 specifications. Defect sensitivity for the NIST – ATP / KLA-Tencor is reaching toward 65nm. Also further developments are needed in CTE to meet "Class A" of +/-5 ppb/ ^{o}K (w/ variation of 6 ppb/ ^{o}K), defect metrology to meet 50nm PSL, and overall flatness. The good news is that square format LTEM substrate materials are commercially available from at least three suppliers.

3) Don Sweeney (LLNL / EUV-LLC) – EUVL Mask Mutlilayers

Don reviewed the status of the EUVL mask blank multilayer deposition and related repair strategy developments. The LLNL facilities has two separate Moly / Silicon Ion Beam sputtering tools in which EUV M.L.s have been producing mask blanks. The EUV mask requirements are integral to the overall exposure system since the mask is reflective it can be viewed as one of the optic surfaces in the exposure tool optic train. Therefore the need for the EUV M.L. control and matching to the exposure tool optics is pivotal. It must support an overall 1% illumination uniformity control at the wafer exposure level. The LLNL mask blank activity has been significant with more than 50 square blanks delivered to the LLC members in over a 5-month period. The added defects in the M.L. deposition process appear to be the most critical issue related to the mask as buried defects can cause phase defects due to M.L. build-up around the defect. The requirement of meeting / exceeding 0.0025 defects / cm2 essentially means there is to be 0 (zero) defects within the quality area. The current level of performance for added defects is 0.04 def./cm2 (>90nm PSL equivalent) with the best blank to date measured at 0.01 def./cm2. Don showed the experimental results of different defect mitigation / repair strategies that could offer leverage against the demanding 0.0025 def/cm2 requirements. Defect smoothing is a candidate strategy with experimental results showing that resulting defect heights at the top surface from a buried 50nm diameter defect can be reduced to 6.5nm heights. By adding an additional ion etching at non-normal incidence, smoothing can further be reduced at the surface to 1.0nm heights. Another strategy is to use focused electron beam to heat the moly/silicon layers which causes local contraction of the M.L. impacted by the buried defect and thus produces a smoothing effect. Ion Milling is another strategy to repair defects found on the top or upper M.L. surfaces. The Ion milling actually removes a few of the M.L. in the area where the defect once was. A slight phase shifting or change in refractive indices of about 3% results.

4) Pei-Yang Yan (Intel) – EUVL Mask Patterning

Pei-Yang reviewed the status of the EUV mask patterning developments including work from Intel, Infineon, IBM, and Motorola. Considerable focus was devoted in reviewing the absorber, buffer, and their reparability characteristics of the leading candidates. Chrome (Cr) and Tantalum Nitride (TaN) offer attractive absorber performance giving high absorption, chemical stability, clean ability, good etch pattering, as well as others. The leading buffer candidates of SiO_2 and SiON provide low absorption, low ion sputtering, increased inspection contrast vs. absorber, and others. Pattern inspection measurement with optical tools (i.e. 257nm DUV) is highly desirable and absorber materials listed above provide good

image contrast greater than 50%. Pei-Yang also showed the successful fabrication of 16 square format EUV masks at Intel to support ETS and other experiments. Minimum feature size down to 30nm node with very good square sidewalls were seen on these masks. Motorola has produced 100nm node CMOS device pattern square EUV masks with CD uniformity of +/- 10% and minimum resolution of 320nm (at the mask). Both the MCoC / IBM and Infineon have also demonstrated square mask EUV fabrication with both Cr/SiO2 and TaN absorber / buffer materials. The further development needed to support 2005 tools for process developments are substrate flatness and defect inspection, mask blank defect inspection and new M.L. coating tools, as well as new repair tooling capability with higher etch selectivity and EUV AIMS tooling.

5) Alan Stivers (Intel) – EUVL Mask Defect Strategy

Alan reviewed the inspection and repair strategy for substrates, blanks, and pattern EUV masks. Alan showed the impacts to embedded defects in the ML on CD control (e.g. 20% CD change on 25nm line caused by a 65nm diameter x 1.5nm high bump). There is the need to find these defects at the blank inspection due to issues with the patterned mask defect inspections not being able to pick up the embedded ML defects. Although pattern inspection can utilize optical tools there is the need for EUV AIMS type tool for locating ML defects. Alan outlined the pattern inspection tooling timing that supports 65nm node "pilot" needs by '03 driving towards 45nm node development capability by '05 and production phases by '07. Defect mitigation strategies were reviewed to compensate for lower yield mask blanks (higher defect counts). Possible strategies included mask blank sorts, defect aligning, defect proximity correction, defect proximity repair. Depending on the location of the defect with respect to absorber sidewalls may dictate whether that defect will print or not. Implementing the mitigation strategies together will decrease the printing of these defects. Alan showed further detail of the Defect Proximity Repair (DPR) strategy which employs FIB trimming of the absorber that compensates for the aerial image / reflectivity loss. SEM photos of absorber trimming were shown on the mask vs. the resulting printed features at the wafer demonstrate the elimination of defect printing. For these strategies to be fully realized significant tool developments are required that include defect size requirements (30nm PSL sensitivity), EUV AIMS tooling for defect locations / mapping, as well as optical pattern inspection tooling developments in reflectivity algorithms and reflected light database S/W.

6) Barry Lieberman (Intel) – EUV Mask Development / Commercialization Infrastructure Dev.

Barry reviewed the approaches needed to develop proper EUV mask tooling to meet the EUV technology requirements. There were three distinct categories of tooling that were outlined in relation to how much development and innovation is required. Category #1 are tooling that can be extensions of current technologies used for optical masks. Hard defect patterned inspection, soft defect inspection, as well as writing and etching equipment fall into this category. Patterned (Hard) defect inspection tooling will require improvement in sensitivity to 50nm by 2005 with higher NA and smaller wavelength sources needs. Soft defect inspection, also a "category #1" tool, can take the form of actinic or non-actinic approaches. The non-actinic has the current development roadmaps for EUV application and can leverage off current pattern inspection platforms. Category #2 type tools are described as those technologies which core technology exists but the requirements are unique to EUV compared to optical masks. These tools are mask repair with gallium staining issues if conventional FIB is used, Aerial Image Metrology (AIMS) where EUV specific source wavelength, optics and environment is significantly different that it's optical counterparts, and flatness metrology. Category #3 tooling is defined as technology where invention or significant extensions are required. Blank inspection and soft defect inspection using actinic inspection that needs scalability to 30nm defect sensitivities and TPT improvements fit into this "Category 3". A strong coordination in three areas is needed to ensure timely mask availability. These are mask piloting activity, concurrent engineering between exposure tool and mask suppliers, as well as including the EUV mask developers as collaboration partners in the EUV technology development.

7) Frank – Michael Kamm (Infineon) – EUV Mask Dev.: Pilot Line at Infineon

Frank Michael reviewed the Infineon / IMS joint EUV mask pilot line. Within this line are three writers (Leica SB350, Etec Alta, and Toshiba EBM), etchers / pattern transfer (Plasmatherm SLR 770 & AMAT), as well as core metrology / inspection tooling including Leica LMS IPRO, KLA CD –SEM & KLA SLF 77. A suite of repair technology tooling is also present. SEM photos were shown to demonstrate the pilot line capability with resist imaging and pattern / absorber etching. Infineon / IMS line has data that shows that the processing of EUV masks can have both reflectivity loss and peak wavelength shifts which are being investigated further by looking into etch depth, contamination, and thermal loading impacts as causes.

Frank – Michael showed substantial data that characterized the performance of the pilot line inspection tools with regard to EUV masks. Defect size calibration between the KLA SLF and SEM was shown. Reflectivity impacts from different capping layers and their thickness were shown. Silicon tends to show better performance versus Zr and Ru due to smaller absorptions and smaller interference oscillation. Stress control and stress related impacts on image placement were shown. This supported the need for ML stress control to be maintained at an 8 MPa precision to support a 1nm IPD control. A maximum of 4.8nm IPD variations can be seen with a 40MPa M.L. stress change over a full mask area (using a 3-point chuck). The Infineon / IMS EUV mask pilot line demonstrates flexible processing with various materials, successful processing both on optical writers as well as 50 kEV e-beam tools, as well as significant work done to understand reflectivity / imaging performance of capping materials and ML stress control needs.

8) David Walker (Photronics) – Commercialization of EUVL Masks at Photronics

David showed the results from the Photronics / IBM MCoC joint efforts since 1999 as well as the EUV masks made to support the EUV-LLC. CD control results from the ETS mask test reticles were shown that supports a 15nm (3 sigma) CD variation for a 50nm node (i.e. 200nm mask feature) specification. Detailed SEM photos showing dense lines / spaces for 200nm features with 1:1 and 1:2 duty cycles as well as 240nm contacts shows very goods image quality and CD uniformity. The MCoC also produced masks having 45nm node SRAM designs based on a 1Gigabit system. Here a 184nm CD mean with uniformity control of 13nm (3 sigma) was achieved using an IBM KRS resist process. David showed the contrast curves for different absorber and buffer films for pattern inspection that supports sufficient contrast levels (>40%). Significant amounts of work were shown that supported mask defect inspection using programmed defects. Again the need for defect density improvements was shown with the NIST ATP measurements on ULE pre and post M.L. coated substrates that reached defect densities of 178 def./cm2. The developments at the MCoC supports EUV mask capability for the 70nm node needs by mid 2005 and the 50nm node needs by mid 2006. David further reinforced the need to have better low defect mask substrates, definition of the absorber & buffer stacks, and definition of mask holding in the mask fabrication process. The MCoC is also supporting EPL mask developments.

9) Scott Hector (Motorola) – Modeling the Cost of EUVL Masks

Scott reviewed the improved Cost of Ownership studies on EUV mask blanks as well as finished patterned EUV masks with the introduction of defect mitigation strategies. Using the baseline CoO assumptions from previous studies a Poisson yield model dictates a ML deposition yield of 60% for a defect density of 0.0025 def/cm2 and a 0.005 def/cm2 total defect density level (native plus adders). This drives an EUV mask blank cost of ~$6,300. Scott demonstrated the mask cost impacts with the ability to relax the defect density requirements and implementing defect mitigation strategies such as e-beam repair and FIB repair. The resulting final mask prices (2 times the process cost assumption) could range from $47,000 up to $88,000 depending on incoming LTEM substrate costs, defect density allocations, and pattering yield with defect repair. These prices are reasonable given calculated 157nm optical binary masks are at $50,000 or PSM reticle sets (complementary pair) calculated prices of up to $100,000. Scott reviewed the expected learning rates needed to support 60% M.L. defect yields with the impact of introducing new technologies by 2007.