

SEMI Standards for EUVL Masks

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Summary of July 23, 2002 SEMI EUV Mask Task Force

- **38 attendees from 28 companies or organizations signed in.**
 - Blank suppliers represented included Corning, Heraeus, Hoya, SESO and Xenocs.
 - Mask users attending included AMD, Infineon, Intel, and Motorola.
 - Mask equipment suppliers included ADE Phase Shift, Agilent, Electrogrip, Incam Solutions, Invax Technologies, KLA-Tencor, Leica, Mykrolis, QED Technologies, Spectral Technology and Toshiba Machine.
 - Exposure tool suppliers represented included Canon and Nikon.
 - Mask suppliers represented included DNP.
 - ASET, EUV LLC, ISMT, Lawrence Livermore National Lab, NIST and University of Wisconsin were represented.
- **Proposed changes, including 3499 ballot results, to SEMI P37-1101 for EUV mask substrates were reviewed.**
 - A proposed specification for free form flatness was presented.
- **The ballot results for and comments on the technical ballot on draft 3414 for EUV mask blanks were reviewed.**
 - The ballot tally appears to be sufficient to publish the standard, but many comments need to be addressed.
- **A draft standard for chucking 3419 was reviewed.**
 - No opposition was raised to the present approach, but many suggested for improvements were provided.
- **The status of standards for reticle storage and handling (3553) was briefly reviewed.**



Summary of October 14, 2002 SEMI EUV Mask Task Force

- **40 attendees from 22 companies or organizations signed in.**
 - Blank suppliers represented included Corning, Hoya, SAGEM, Schott Lithotec, Tosoh and Xenocs.
 - Mask users attending included AMD, IBM, Infineon, Intel, and Motorola.
 - Mask equipment suppliers included Leica, QED Technologies and Toshiba Machine.
 - Exposure tool suppliers represented included ASML, Canon and Nikon.
 - Mask suppliers represented included Photronics.
 - ASET, EUV LLC, ISMT, LBNL, LLNL and University of Wisconsin were represented.
- **Proposed changes to SEMI P37-1102 for EUV mask substrates were reviewed.**
 - A proposed change to the definition of CTE was presented by Corning.
 - A proposed change to the local slope and HSFR requirements was presented by LBNL.
- **Proposed changes to SEMI P38-1102 for EUV mask blanks were handed out but not reviewed. Proposed changes will be reviewed by email.**
- **A draft standard for chucking (SEMI draft 3419) was reviewed.**
 - Significant discussion surrounded the rationale for the standard.
 - University of Wisconsin presented modeling results on the effect of pin spacing, pin coverage and effective conductance on in-plane distortion of chucked EUV masks.
 - ASET presented that a 3-point mount was preferred in the e-beam, but they also stated the requirements for an electrostatic chuck in the e-beam system that would also satisfy the mechanical requirements of draft 3419.
 - ASML provided a revised layout for Figure 1 with a proposed 26 by size limit.



Agenda

October 14, 2002 (1-5 PM CDT)

The Spectrum room at the Intercontinental Hotel in Addison, TX (Dallas area)

1 - 1:30 Introduction

1:30 - 1:45 Discussion of proposed modifications to SEMI P37-1102 (substrates)

1:45 - 2:00 CTE specifications (Ken Hrdina of Corning)

2:00 - 2:15 Spatial frequency requirements for local slope and HSFR (Gullikson)

2:15 - 2:45 Discussion of proposed modifications to SEMI P38-1102 (blanks)

2:45 - 3:00 Break

3:00 - 3:15 Discussion of SEMI draft 3419 (chucking)

3:15 - 3:30 Pin spacing requirements (Mikkelson of Univ. of Wisconsin)

3:30 - 3:45 Comments from of ASET (Ogasawara-san of ASET)

3:45 - 4:00 Comments from ASML (Brian Blum of ASML)

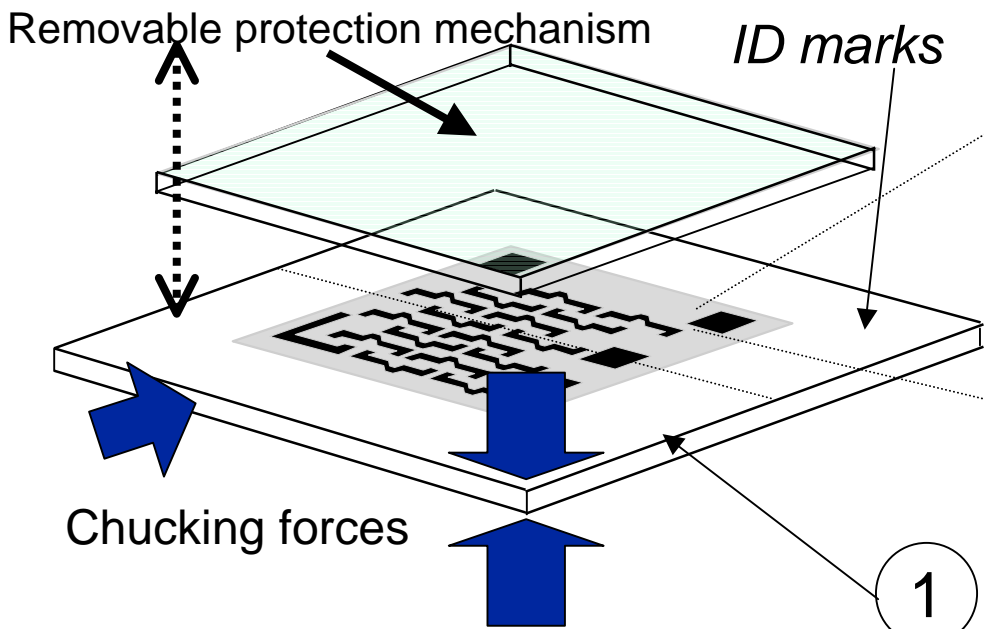
4:00 - 4:30 Discussion



EUVL mask standards

4 Storage container and attributes of removable protection mechanism (3553)

ASML drafting proposal;
ISMT formed working group

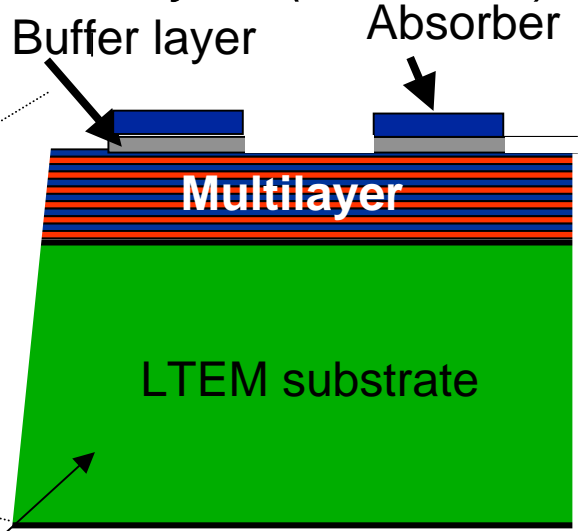


2 Chuckling in processing and exposure tools, location of ID and alignment marks (3419)

Preparing informational (blue) ballot by 1/

3 Proposed revisions being discussed

Multilayer coating material, absorber and buffer layers (P38-1102)



Cross-section of EUVL mask

1 Mask substrate (P37-1102)

First revision completed. Further revisions are proposed, but they might need to wait for establishment of chuckling standard.

Become voting members of SEMI

- **Participants in EUV Mask Task Force meetings are requested to become voting members of SEMI Microlithography.**
 - See www.semi.org
- **Anyone can become a voting member, but only one vote is tallied from each company or organization.**
- **To help gain a quorum on EUV mask ballots, which requires 60% of voting membership to cast a vote, a greater population of members interested in EUV is needed.**

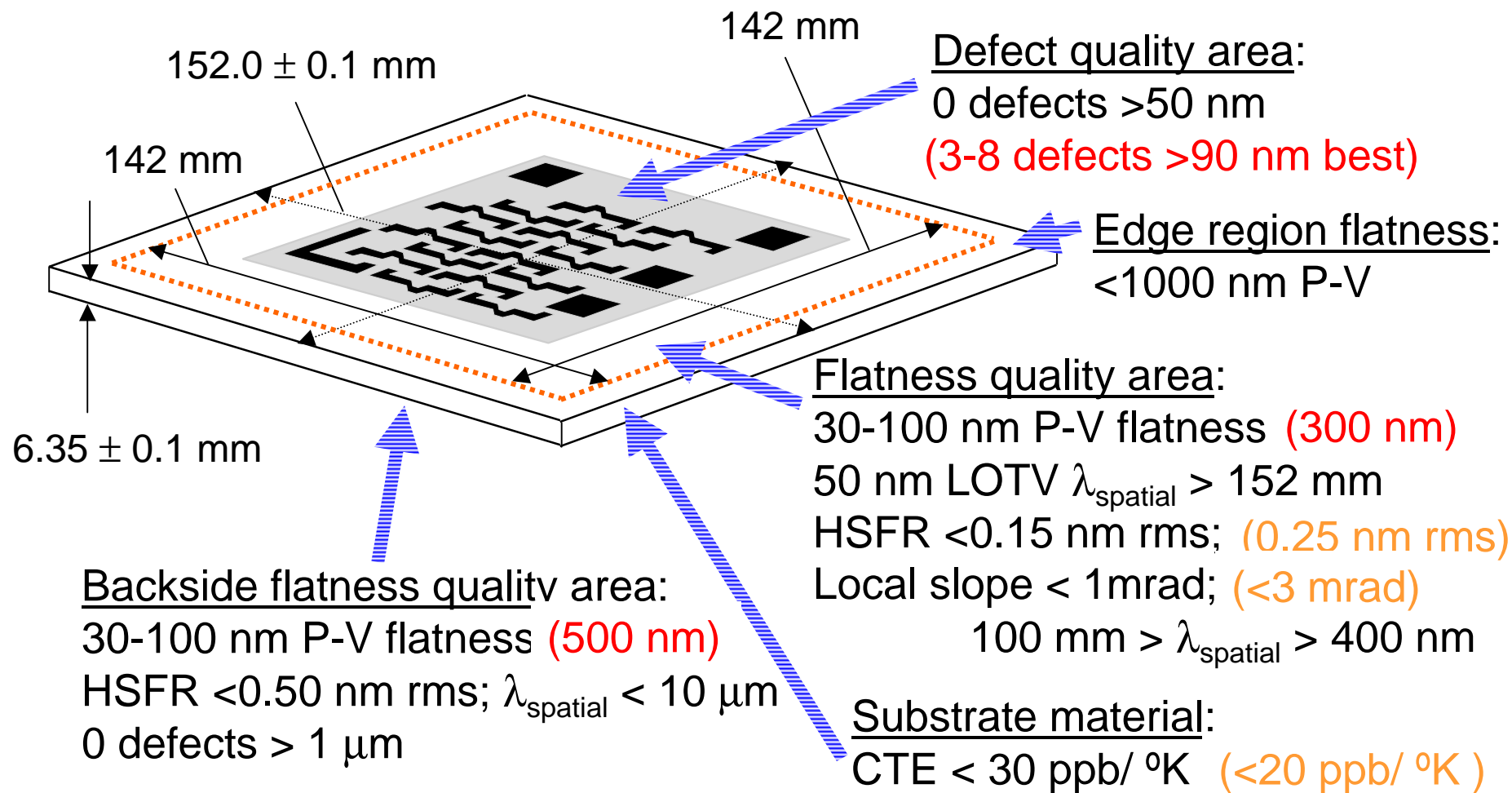


Discussion of SEMI P37-1102

**SPECIFICATION FOR EXTREME ULTRAVIOLET
LITHOGRAPHY MASK SUBSTRATES**



Photomask as EUVL mask form factor takes advantage of existing mask infrastructure



SEMI standard P37-1102

5 suppliers have delivered a total of 133 mask substrates to the EUV LLC.*

Possible revisions of SEMI P37-1102

- **Change order of classes for flatness**

D 30 nm, C 50 nm, B 75 nm, A 100 nm

In standard P37-1102 in reverse order to allow more aggressive values if needed

Other class values are not in reverse order. Make class order consistent.

- **Review and modify spatial frequency requirements on flatness**

- Consider allowing for free form flatness errors of mask substrate in addition to wedge and thickness variation.
 - Free form flatness error = $(\text{front} + \text{back} - \text{wedge}) / 2$
 - A proposal to use a basis set such as Legendre polynomials to characterize free form flatness errors will be considered.
- Consider relaxing backside flatness requirement if permitted by chucking approach.
- *Status: awaiting chucking standard. Free form flatness specification proposals are under review.*



Possible revisions of SEMI P37-1102 (cont.)

- **Relax dimensional tolerances somewhat**
 - Increase tolerance on edge length to 0.2 mm from 0.1 mm
 - Increase squareness from 0.01/25.4 to 0.04/25.4
 - Relax tolerances on rounded edge or camfer dimensions by ~2X
 - Change the locations where the notch is dimensioned
 - *Status: awaiting proposed mask storage and handling standard which might be affected by dimensional tolerances*
- **Review datum locations and use**
 - Films added to substrate might affect the use of the datum surfaces
 - Datum approach intended to avoid the use of physical marks
- **Include fiducial marks on the front of the substrate to aid in defect location registration**
 - Proposed location is near the edge with ~0.5 micron depth
 - Laser marks might cause chipping or serve as a location for defects to cluster
 - *Status: need experimental data on defects caused by marks (if any)*
See presentation by Jim Folta. So far, no convincing data is available that adding etched ID marks increases defect levels, but no data is yet available for etching marks into a glass EUV mask substrate.
 - *Incorporate learning from draft 3133 in the SEMI Traceability Committee*

Possible revisions of SEMI P37-1102 (cont.)

- **Modify standard to allow for low order Legendre modes in flatness error**
- **Change CTE specification to use ASTM E228-95 standard definition of mean CTE (see Corning presentation)**
 - Check whether slope of CTE with temperature needs to be specified
 - Specify maximum temperature of substrate during fabrication of mask or its use
- **Modify specification on local slope and HSFR as follows:**
 - Reduce the frequency range on the HSFR specification to:
 - $4 < f < 20 \text{ mm}^{-1}$ (no smoothing) or
 - $4 < f < 10 \text{ mm}^{-1}$ (typical for ion beam deposition).*
 - Adopt an RMS slope specification for frequencies $< 3.5 \text{ mm}^{-1}$.

| Mask Error | Tolerance | Frequency Range (μm^{-1}) |
|--------------|--------------|--|
| Flatness | 50 nm P-V | |
| Slope (low) | 0.2 mrad rms | $0.001 < f < 0.5$ |
| Slope (high) | 0.4 mrad rms | $0.5 < f < 3.5$ |
| HSFR* | 0.15 nm | $4 < f < 20$ |

* Ultimately could be decided between substrate and coating vendors.

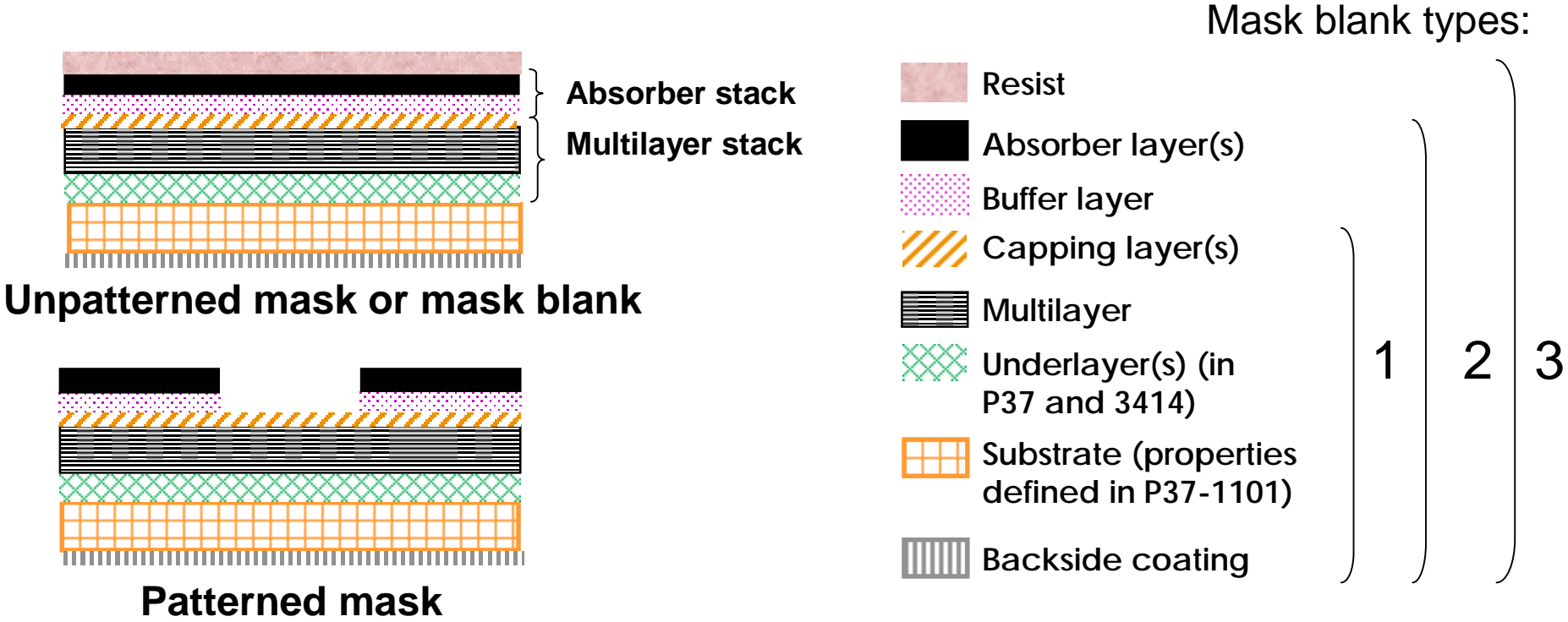


Discussion of SEMI P38-1102

**SPECIFICATION FOR ABSORBING FILM STACKS
and MULTILAYERS ON EXTREME ULTRAVIOLET
LITHOGRAPHY MASK BLANKS**



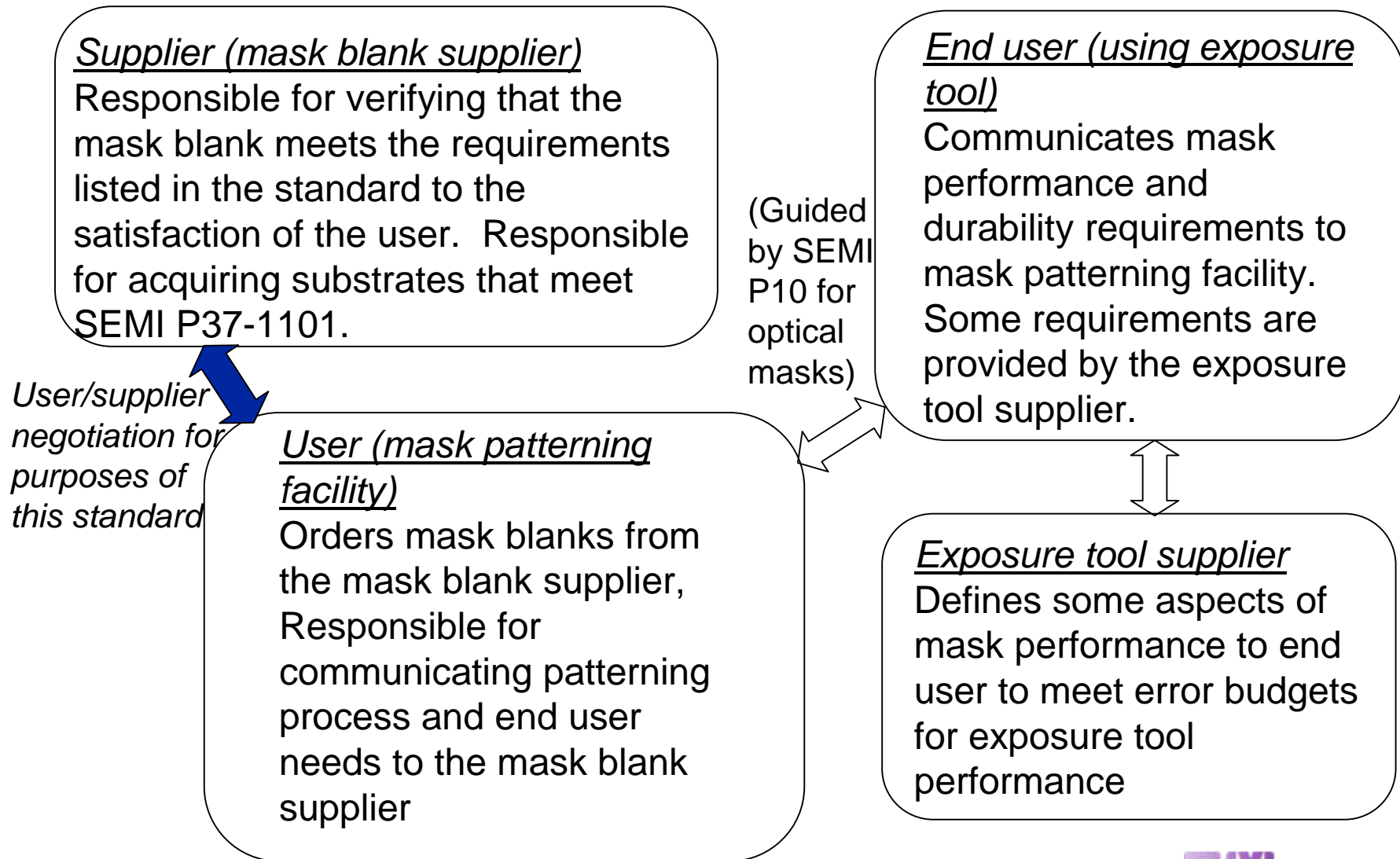
Overview of mask absorber and multilayer standard (SEMI P38-1102)



- Lists all parameters of the *mask blank coatings* that user and supplier need to define for mask performance, including patterning requirements
- Consider needs for mask absorbers and multilayers through the 22-nm half pitch ITRS node



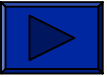
Relationship model for ML/absorber standard



Proposed revisions of SEMI P38-1102

- **Require a conducting path between the front and backsides of the mask blank.**
 - E-beam lithography requires that the front surface of the mask be grounded.
 - The use of thermophoresis for mask protection from defects requires that the front surface of the mask be grounded.
 - Grounding front to back will require the ML or other conducting layer to extend to edge
 - *Task Force: Add this item into the ordering information but leave it up to the user and supplier to negotiate the details.*
- **Possible international standard for multilayer coating median wavelength**
 - *Task Force: EAPSMs used today require many different types of mask blank coatings for different users. Since a source choice has not been made and tool designs are in early development, this issue will be addressed in the future if the users and mask blank suppliers raise it as a concern.*



Proposed revisions of SEMI P38-1102 (continued)

- **Change the footnote in Table 11 from “** At 30 degrees with respect to normal to the absorber surface” to “** At normal incidence** 


 - Better define what is meant by normal incidence in the text
 - *Normal incidence is the preferred value.*

- **Need to add a requirement for uniformity of reflectivity at the inspection wavelength**
 - Initial proposal is $\pm 1.5\%$ range
 - *Requirement probably not needed if absorber stack reflectivity $< 10\%$*



Proposed revisions of SEMI P38-1102 (continued)

- **In Table 10/11: An alternative would be to define the reflectivity values at one specific inspection wavelength, which shall be agreed upon between user and supplier.** 
 - Some materials might be excluded if they do not fulfill the reflectivity properties over the whole specified range (150 – 257 nm), even if they would be appropriate for the selected inspection wavelength.
 - Text can be added in Sections 7.2 and Sections 7.4 to accommodate this option.
 - Propose that range of inspection wavelengths is reduced to 193 to 257 nm.
- **In Table 9, depending on attributes, some properties refer to the absorber stack only (stress,...) and others to the global stack (reflectivity,...) for a better understanding it would be better to indicate this in the table.** 
 - This might be noted where appropriate using a footnote.

Proposed revisions of SEMI P38-1102 (continued)

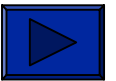
- **In Table 9, "Stress change" should be specified as an absolute value of this attribute that has to be below the limit**
 - This change should be made to allow both an increase or a decrease in stress. 
- **Reconsider the requirement for 50 MPA stress change after 50 billion pulses.**
 - This requirement might be too demanding and too difficult to test.
 - @10 kHz, ~800M pulses per day; 50B = 140 days
- **Figure 4 should refer to the EUV reflectivity definition (wavelength and angle) to Section 12.2**
 - A reference to Section 12.2 can be added to the caption of Figure 3.

Proposed revisions of SEMI P38-1102 (continued)

- **Secondary electron contrast properties defined in Table 7 apply to the entire stack of materials since the underlying layers may contribute to this property (at least at higher acceleration voltages.** 
 - This might be noted with a footnote.
- **Eliminate secondary electron contrast properties from Table 7 to not drive absorber stack material choice with this parameter** 
- **Add 1% absolute to all reflectivity values in Table 5**
 - Allows for 1% reflectivity loss due to the patterning process while still meeting the ITRS requirements for the 32-nm node

Proposed revisions of SEMI P38-1102 (continued)

- **Add another Type 4 to Table 1 without a backside coating.**
 - This would allow the option of applying the coating after mask processing.
 - The coating might be required for pattern generation lithography if the draft 3419 chucking standard is adopted.
 - There could be three combinations of this proposal if it is made an option for any of the three mask blank types in the standard. Should we add three more types? Maybe we could make the backside coating layer optional if permitted by draft 3419.
- **Add class E (test) for >90 nm defect size into Table 13**



Proposed revisions of SEMI P38-1102 (continued)

- **Add an additional row to Table 12**

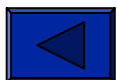


Areas of conductive coating Agreed upon between user and supplier.

- This option would allow for an introduction of a backside exclusion zone, which might become necessary if contact with the backside layer creates unacceptably high particle levels during handling.

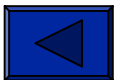
- **In Table 15, specify which type of labeling should be used. Should the information be etched in to a blank layer or the edge, or should it be printed on the box?**

- The present standard allows either option.



Proposed revisions of SEMI P38-1102 (continued)

- **Include a requirement on the thickness of the backside layer so that its resistivity divided by its thickness is greater than 2 Ohms to prevent significant eddy currents in the e-beam writer**
- **Change Section 4.2 to read:**
 - "Resist system – Layer of radiation-sensitive material with an optional hardmask layer between the radiation-sensitive material and the absorber material. The radiation-sensitive material is patterned in the lithography process for fabrication the mask."
 - P38-1102 allows a hardmask because in Section 4.3, one or more layers are permitted for the absorber layers.



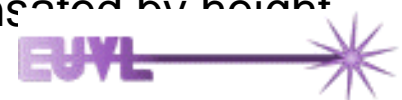
Discussion of SEMI draft 3419

SPECIFICATION FOR MOUNTING REQUIREMENTS
AND ALIGNMENT REFERENCE LOCATIONS FOR
EXTREME ULTRAVIOLET LITHOGRAPHY MASKS



Rationale for chucking standard

- **Standard for chucking in:**
 - Pattern generator (e-beam or optical)
 - Pattern placement metrology tool
 - Exposure tool
- **Without compensation, large pattern placement errors relative to ≤ 45 -nm node requirements will occur**
- **Compensation for these errors will be difficult.**
 - Residual error from calculated compensations remains due to errors in measurement of deformation
 - Compensation methods would need to measure the shape of both sides of the mask and predict the position of front surface points after clamping on a flat chuck
- **Provides for further reduction of overlay error terms:**
 - Eliminates placement error term due to stress in absorber stack and due to stress relaxation of multilayer stack
 - Eliminates impact of backside flatness errors on pattern placement
 - LOTV requirement remains but errors could be compensated by height mapping on standard mount



Proposed SEMI standard for mask chucking (draft 3419)

- **Draft standard includes:**
 - Reserved area for overlay alignment marks and ID marks
 - Mounting quality area to be negotiated between user and supplier
 - Standard mask mounting method
 - Bending stiffness $>30,000$ N-m for mask mount
 - Mount local surface flatness error <1 μ rad
 - Clamping pressure 15 ± 0.1 kPa
- **Mask mounting method standardized for:**
 - Pattern generator
 - Pattern placement metrology
 - Exposure tool
- **Status: draft circulated for initial comments on 6/26/02 and reviewed on 7/23/2002**

Terminology

- **Chuck** – The chuck is the physical apparatus in the tools listed in Section 2.1.1 upon which the mask is mounted.
- **Mounting surface** – The mounting surface is the surface of the chuck in direct contact with the mask. The backside of the mask, which is the unpatterned side, shall be in direct contact with the mounting surface while the mask is being used in the tools listed in Section 2.1.1.

Suggestions for modifications to draft 3419 chucking standard

- **Add an additional requirement on maximum chuck pin spacing.**
 - <10 mm pin spacing is an initial value to meet the flatness requirement and not cause large IPD
 - UW will also model a 20-mm pin spacing to verify the <10 mm requirement
- **Consider a requirement on maximum IPD when chucked due to thermal distortion.**
 - This parameter will be determined by the chuck designer.
- **Allow high frequency roughness on the chuck surface to make release from the chuck more rapid.**
 - This parameter will be determined by the chuck designer.
- **Consider a requirement for a stiffness ratio near unity between the chuck surface and the backside coating on the mask.**
 - This parameter will be determined by the chuck designer.

Suggestions for modifications to draft 3419 chucking standard (continued)

- **Section 6.2.1 should better define flatness error**
 - Flatness should be referenced to a best fit plane and defined as the maximum deviation from that plane.
 - Should this flatness be measured before or after chucking?
- **Consider expanding the 3419 draft standard to include the substrate flatness metrology.**
 - Flatness would be measured in the chucked state.
 - Particles between the chuck and the substrate might change the measurement result, so it is also desirable to have a free-standing measurement of the substrate flatness values required by P37.
- **Remove specification of alignment mark locations, etc. from standard at this time (remove 2.2, 5.2-5.5 and Figure 1)**
 - Proposal from ASML with updated layout included in next draft

Suggestions for modifications to draft 3419 chucking standard (continued)

- **Change Section 4.2 to:**

Mounting surface - **The mounting surface is the surface of the chuck in direct contact with the mask. The backside of the mask, which is the unpatterned side, shall be in direct contact with the mounting surface while the mask is being used in the exposure tool, the mask pattern generator and the pattern placement metrology tool.**

- **Combine Tables 2 and 3.**

- Tables separate for ease of future modification using line item ballots.

- **Need to define test methods in Section 7**

- Flatness
- Stiffness
 - Stiffness is a derived parameter, so measurement is not possible
- Clamping pressure
- Test methods will be left up to user and supplier negotiation.

Design parameters of chuck suggested by University of Wisconsin's study

- **Pin coverage**
 - Pin size
 - Pin spacing
- **Effective conductance between the chuck and the mask**
 - Pin height (gap)
 - Gas type
 - Gas pressure
 - Reticle to chuck contact conductance

Proposed modifications to draft 3419 as a result of discussions on 10-14-02 and 10-17-02

- **Replace Figure 1 with new ASML layout**



Old Figure 1

- Field size at wafer limited to 26 by 33 mm
- One of three versions supplied by ASML will be used for blue ballot (see ASML presentation)
- SEMI T11 data matrix could be included

- **Add a requirement for pin spacing**

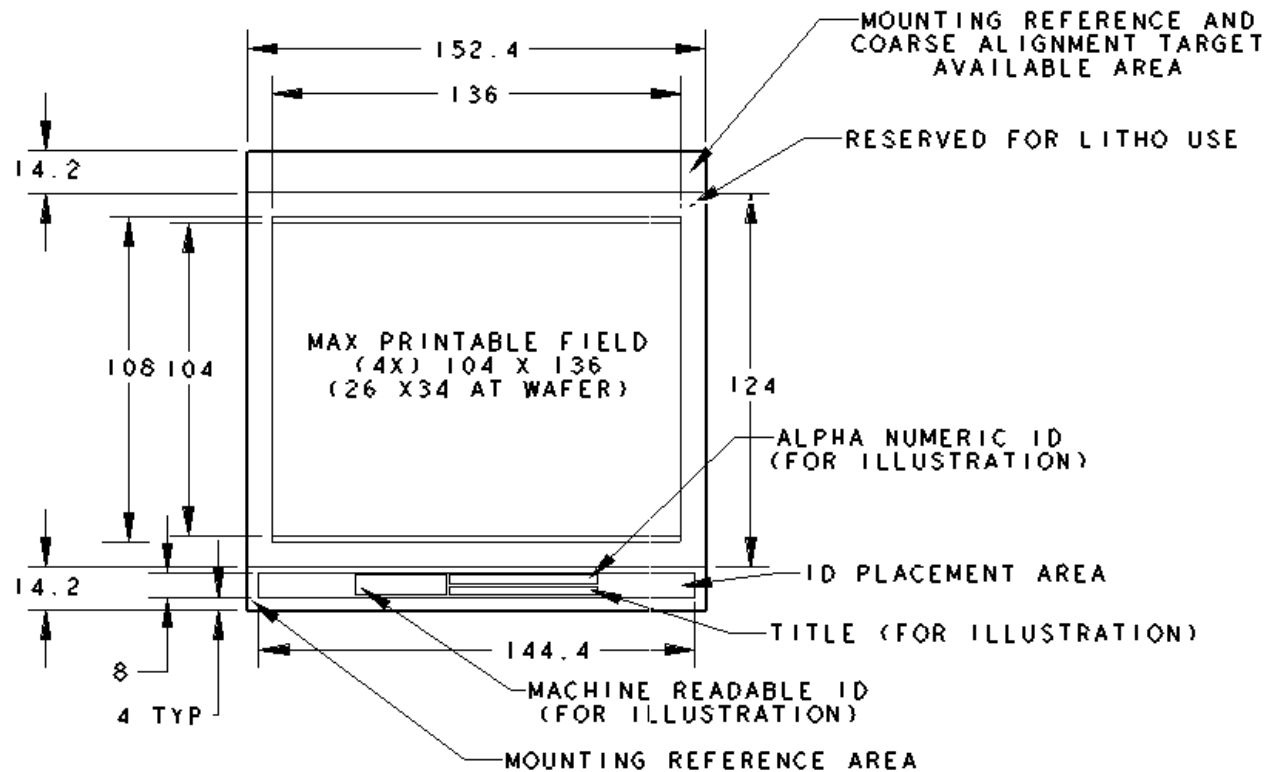
- Change the definition of flatness to allow pins
- Conduct a survey on the need for pins on the chuck
- UW will investigate effects of pin spacing >10 mm

- **Timeline**

- Blue ballot completed by SPIE 2003
- Yellow ballot completed by SEMICON West 2003

Appendix

Proposed mask layout (Figure 1)



- **Provided by SVG in 2000 and might need updating.**



P38-1102 Table 5

Table 5 Peak EUV reflectivity of multilayer stack

| <i>Class</i> | <i>Mean peak reflectivity</i> |
|--------------|-------------------------------|
| A | >67% |
| B | 65 - 67% |
| C | 63 - 65% |
| D | 60 - 63% |

Note: Mean is determined from measurements made at different spatial locations on the mask blank surface. Sample size and measurement locations for determining mean are to be agreed upon between user and supplier.



P38-1102 Table 7

Table 7 Properties of buffer layer

| <i>Buffer layer properties</i> | <i>Requirement</i> |
|--|---------------------------------------|
| Buffer layer etch selectivity to multilayer | Agreed upon between user and supplier |
| Buffer layer material composition | Agreed upon between user and supplier |
| Focused ion beam etch selectivity between buffer layer and absorber | Agreed upon between user and supplier |
| Focused ion beam etch selectivity between buffer layer and multilayer | Agreed upon between user and supplier |
| Secondary electron contrast of the buffer layer with respect to the absorber layer(s) for between 0.5 and 2 kV primary electrons | Agreed upon between user and supplier |
| Secondary electron contrast of the buffer layer with respect to the capping layer(s) for between 0.5 and 2 kV primary electrons | Agreed upon between user and supplier |
| Buffer etch selectivity to absorber stack | Agreed upon between user and supplier |
| Buffer layer thickness | Agreed upon between user and supplier |



P38-1102 Table 9

Table 9 Properties of absorber stack

| <i>Attribute</i> | <i>Requirement</i> |
|--|---------------------------------------|
| Stress | -200 to 200 MPa |
| Mean reflectivity at EUV wavelength*** | <0.5% |
| Uniformity of EUV reflectivity | <0.1% TIR |
| Thickness uniformity | Agreed upon between user and supplier |
| Etch rate in cleaning solutions **** | Agreed upon between user and supplier |
| Thickness change after 50 billion pulses in EUV exposure tool***** | < 1 nm |
| Stress change after 50 billion pulses in EUV exposure tool***** | < 50 MPa |
| Absorber stack outgassing during EUV radiation***** | Agreed upon between user and supplier |

Note: Mean is determined from measurements made at different spatial locations on the mask blank surface. Sample size and measurement locations for determining range are to be agreed upon between user and supplier.*** Reflectivity at 6 degrees angle of incidence with respect to the normal to the absorber surface at the mean median reflected wavelength specified in Table 4 and integrated over the bandwidth equal to the FWHM of the reflectivity versus EUV wavelength

**** Cleaning solutions to be agreed upon between user and supplier

***** 3 to 15 mJ/cm²/pulse in FWHM bandwidth of EUV spectrum



P38-1102 Tables 10-12

Tabl 10 Optical properties of buffer layer and multilayer stack

| | |
|---|---------------------------------------|
| Minimum multilayer stack reflectivity at $150 < \lambda < 257 \text{ nm}^*$ | 55% |
| Buffer layer reflectivity at $150 < \lambda < 257 \text{ nm}^*$ | Agreed upon between user and supplier |

λ is the inspection wavelength

Reflectivity is specified for <1% fractional bandwidth

* At normal incidence

Tabl 11 Optical properties of absorber stack surface

| <i>Class</i> | <i>Absorber reflectivity at $150 < \lambda < 257 \text{ nm}^{**}$</i> |
|--------------|--|
| A | 5% |
| B | 10% |
| C | 15% |
| D | 20% |

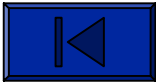
λ is the inspection wavelength

Reflectivity is specified for <1% fractional bandwidth

** At 30 degrees with respect to normal to the absorber surface

Tab 12 Properties of the conductive layer on the back side of the mask substrate

| <i>Conductive layer properties</i> | <i>Requirement</i> |
|------------------------------------|---------------------------------------|
| Thickness | Agreed upon between user and supplier |
| Stress | Agreed upon between user and supplier |
| Mechanical durability | Agreed upon between user and supplier |



P38-1102 Tables 13

Table 13 Defect requirements for multilayer stack

| <i>Class</i> | <i>PSL equivalent size range (nm)*</i> | <i>Maximum defect count</i> |
|--------------|--|---------------------------------------|
| A | > 25 | 0 |
| B | > 30 | 0 |
| C | > 40 | 0 |
| D (Test) | > 60 | Agreed upon between user and supplier |

*PSL equivalent size means the detected defect appears to be the same size as a polystyrene latex sphere examined under the same inspection conditions. Defect count for defects with size smaller than that shown is not specified.

