

International EUV Initiative IEUVI

Paolo Gargini
ITRS Chairman
IEUVI Chairman



2003 Antwerp



Agenda

1. The Three challenges:
 1. Solving the Technical Challenge
 2. Alleviating the Economic Burden
 3. Maintaining Long Term Credibility for a Breakthrough Technology
2. *International EUV Initiative (IEUVI)*
3. Endorsement from the World Semiconductor Council (WSC)
4. Conclusions



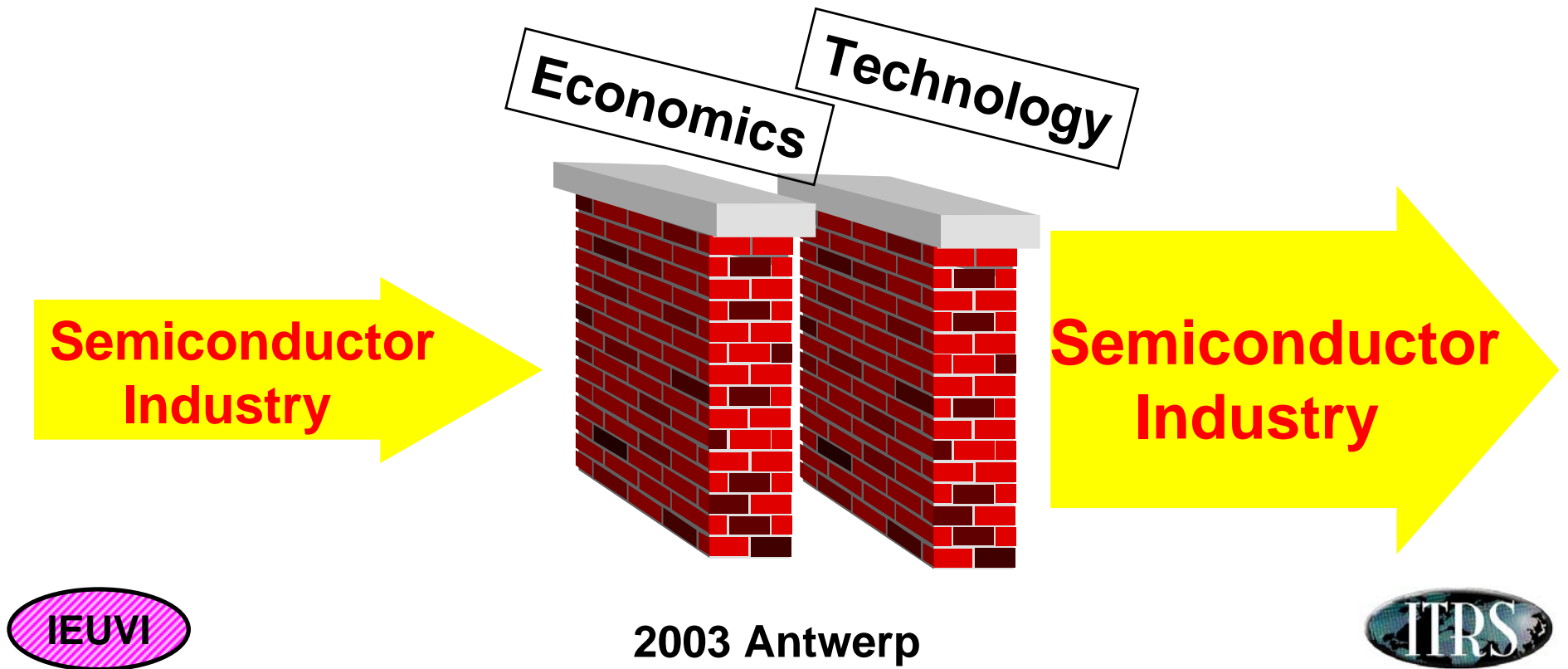
2003 Antwerp



Facing the Double Challenge

90's

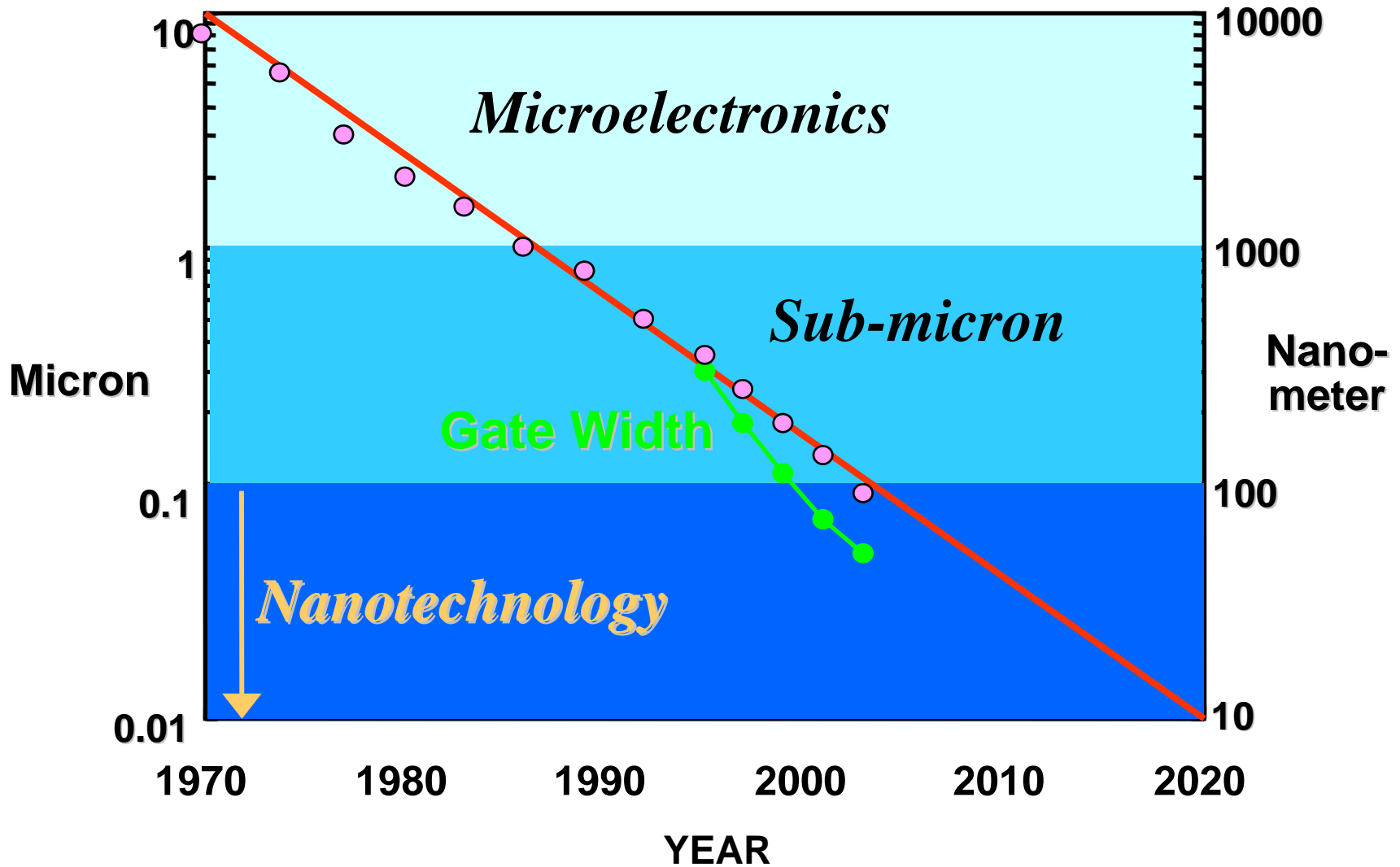
21st Century



2003 Antwerp



Silicon Nanotechnology is Here!



2003 Antwerp



The field effect transistor (FET) can be thought of as consisting of two wells (source and drain) separated by a barrier (channel).

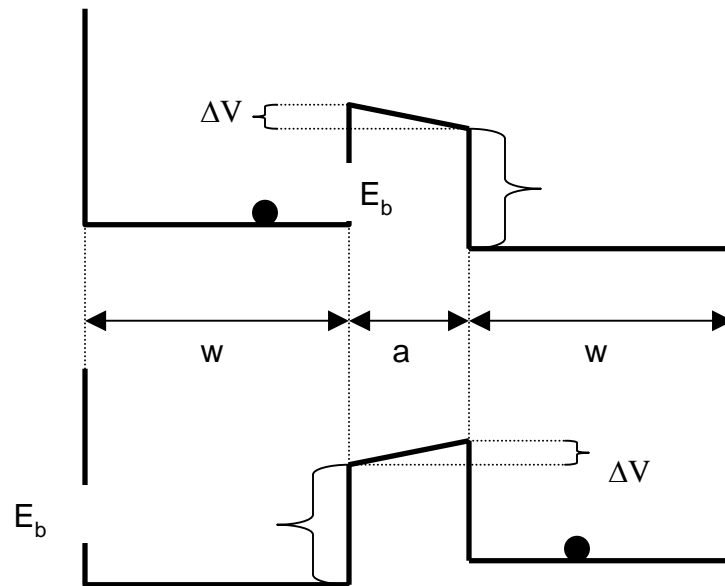


Figure 1. Energy Model for Limiting Device
 w = width of Left-Hand Well (LHW) and Right-Hand Well (RHW)

a = barrier width

E_b = barrier energy,

2003 Antwerp

Performance of the ultimate nanoelectronic device*

- Characteristic dimension $\sim 1\text{-}2\text{ nm}$
- Density $\sim 10^{14}/\text{cm}^{**2}$
- Switching speed $\sim 0.04\text{ ps}$
-but power dissipation $\sim 3 \times 10^6\text{ W}/\text{cm}^2$ -- would vaporize Si instantaneously
- However, if we operate this “device” at 0.17 ps^\dagger and $n = 3 \times 10^9/\text{cm}^2$ †, it dissipates $\sim 50\text{ W}/\text{cm}^2$
- Also, 0.05ps and $n=10^9/\text{cm}^2$ will dissipate 50W

•Assumes room temperature operation, calculation in backup

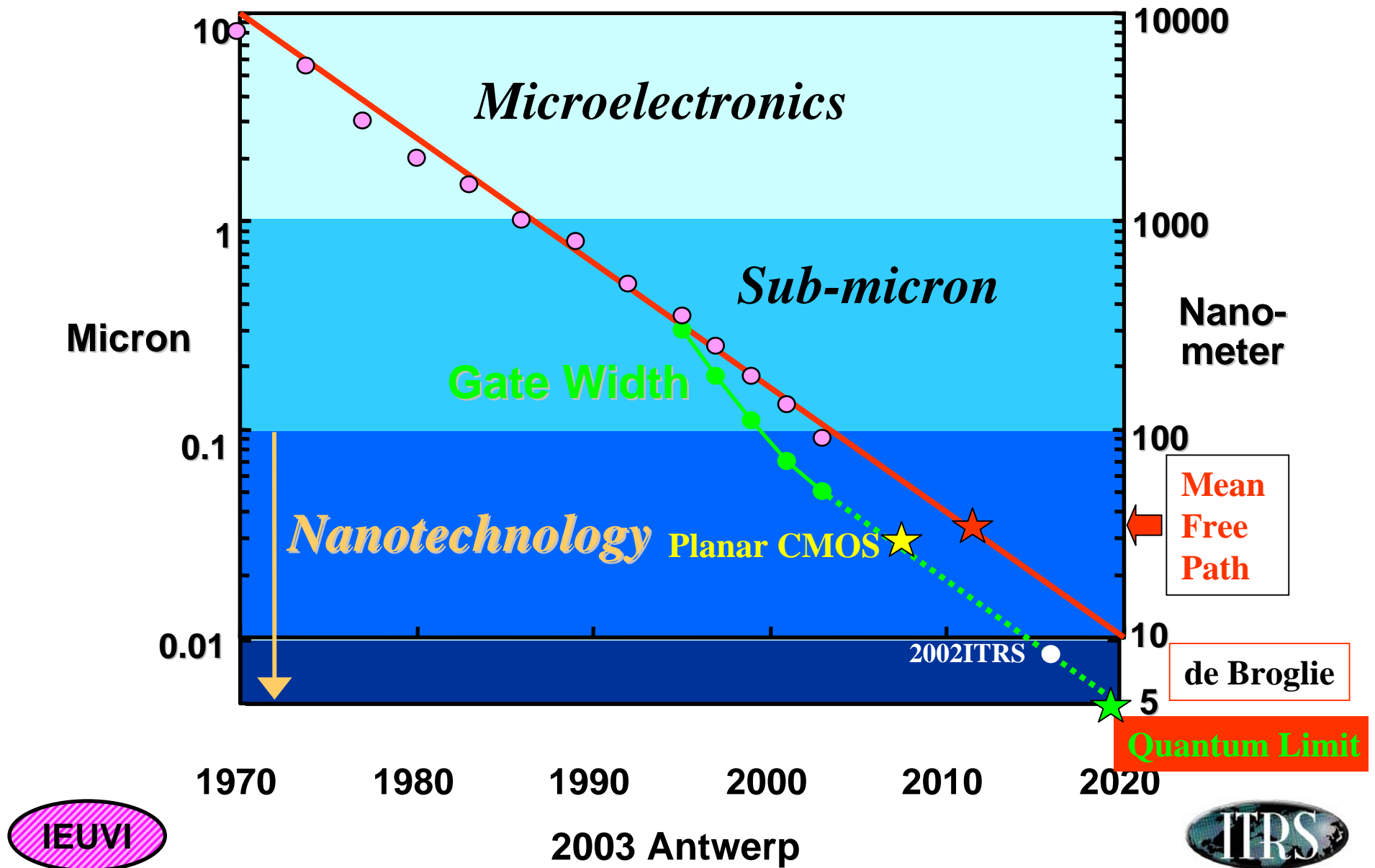
•† Switch speed, device density, 22 nm node, ITRS roadmap



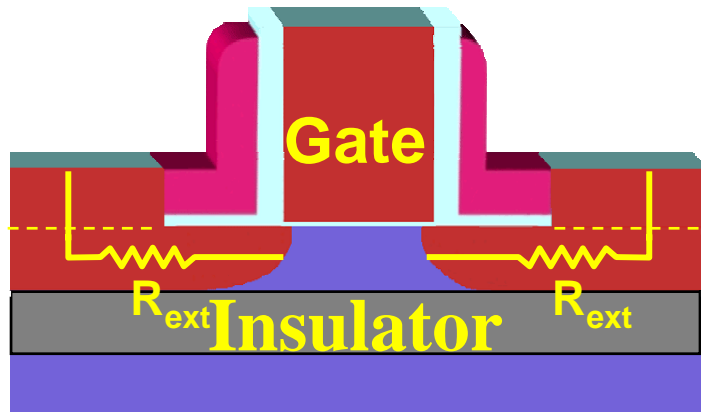
2003 Antwerp



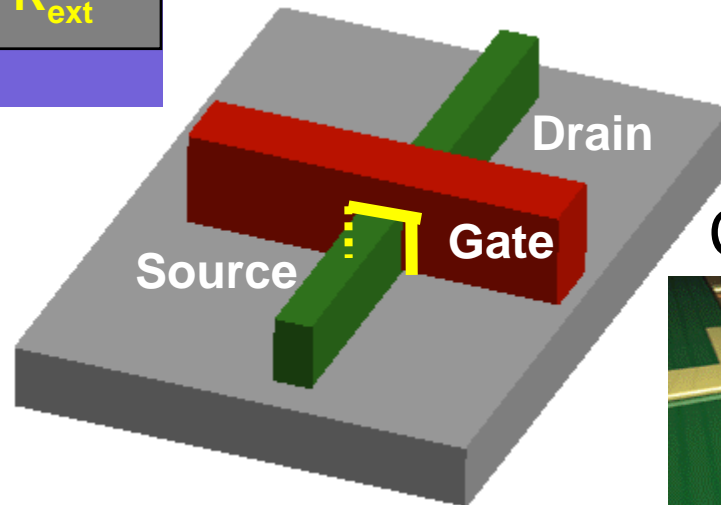
How Long is Silicon Going to Last?



Transistor Evolution

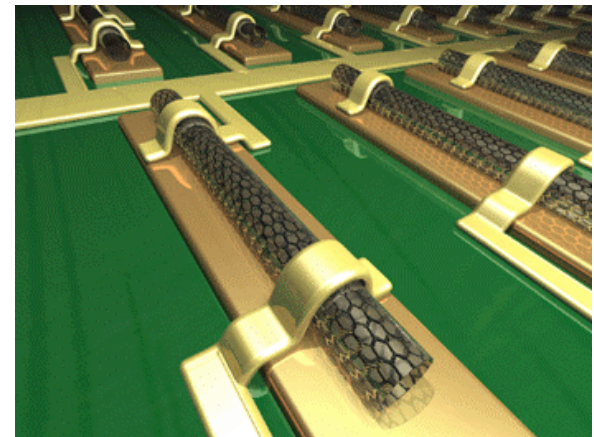


Tri-gate



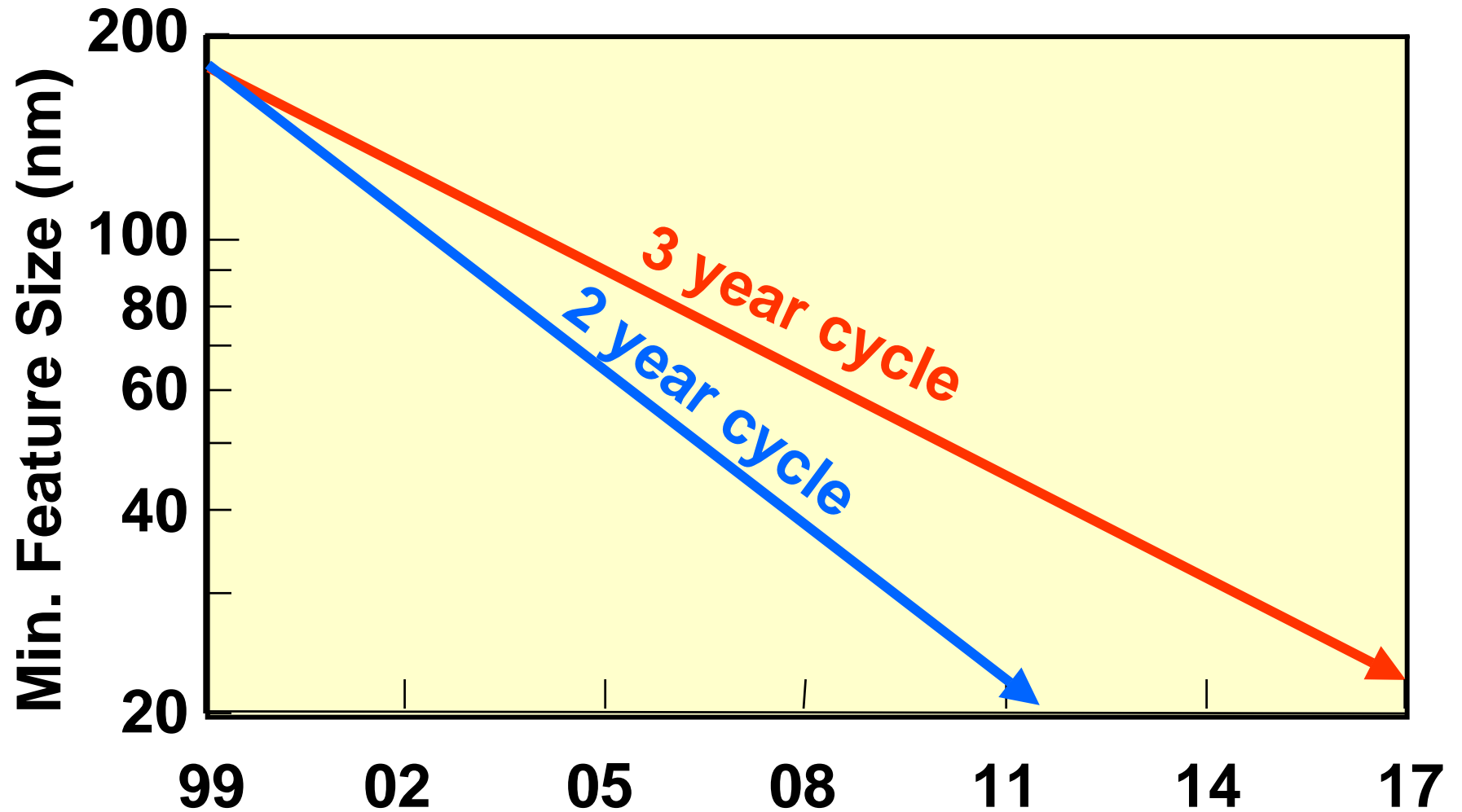
?

Carbon nanotube



Bachtold, et al., *Science*, Nov. 2001

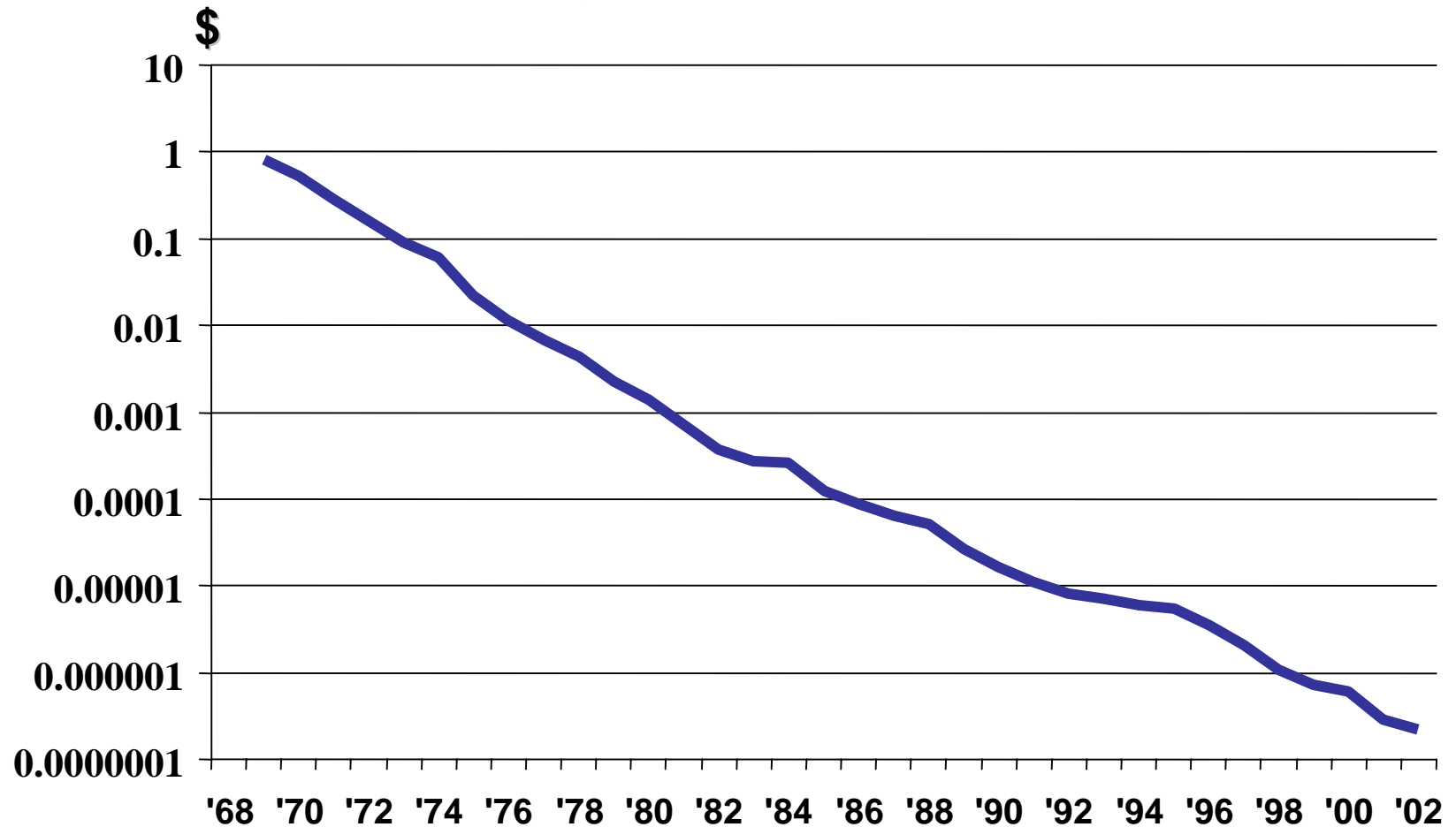
Focus: Return On Investment



Initial production
2003 Antwerp



Average Transistor Price by Year



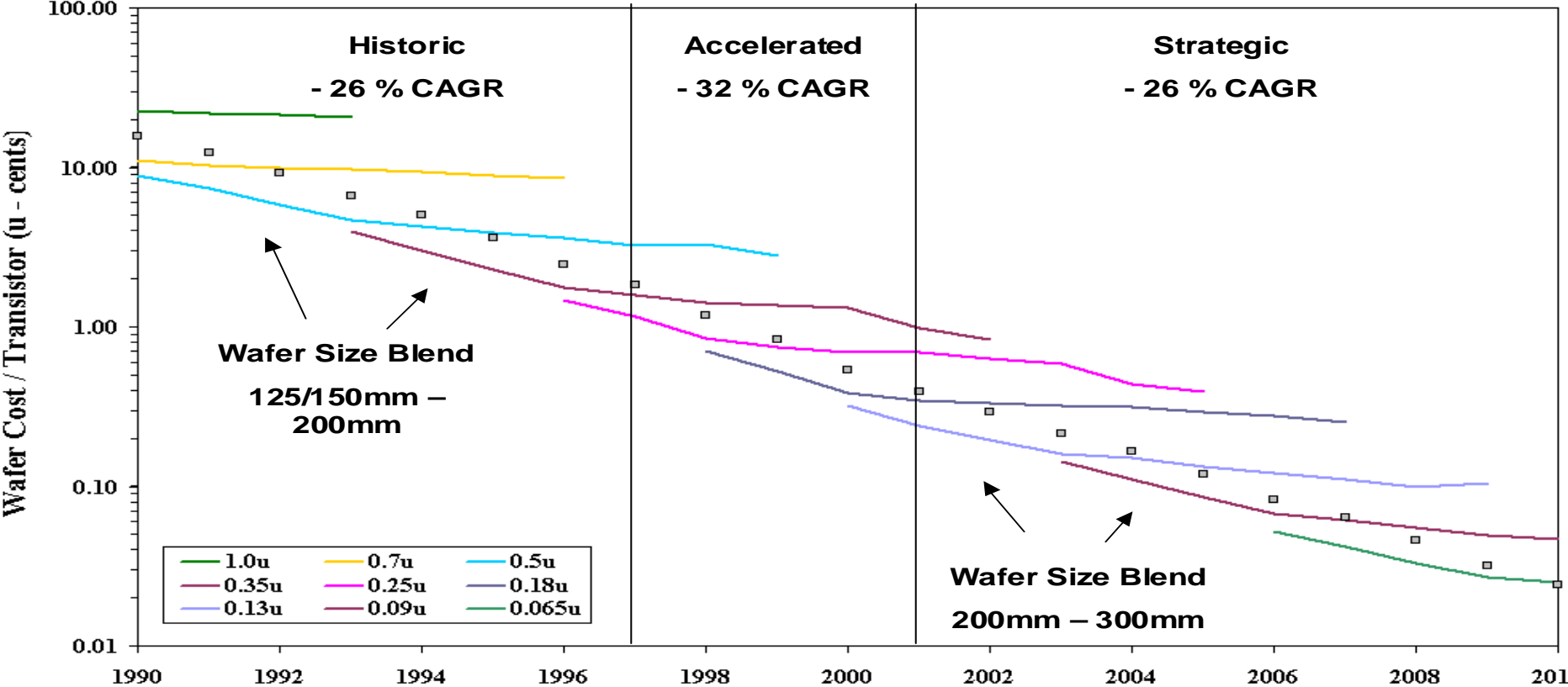
Source: WSTS/Dataquest/Intel, 8/02

2003 Antwerp



Transistor Manufacturing Costs Falling

(Source: Sematech '02)



2003 Antwerp



Rising Fab Cost but Flat per-wafer Cost

	1993	1998	2003
Wafer size (mm)	200	200	300
Fab cost (\$B)	0.9	2	3
Fab capacity (kwpm)	20	40	30 - 35 ~77 (200mm-equivalent)
\$B/kwpm	0.04	0.05	0.04



2003 Antwerp



Facing the Third Challenge: Long Term Credibility

*Can the semiconductor industry fund
a project to success for 20 years?*



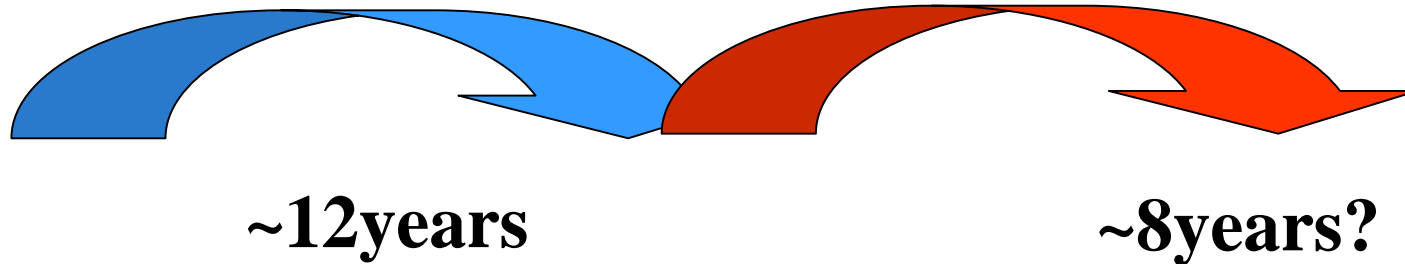
2003 Antwerp



The Road to EUV Commercialization

~1989. Fundamental Patents

Commercialization
(2009?)



2001 ETS Demonstration

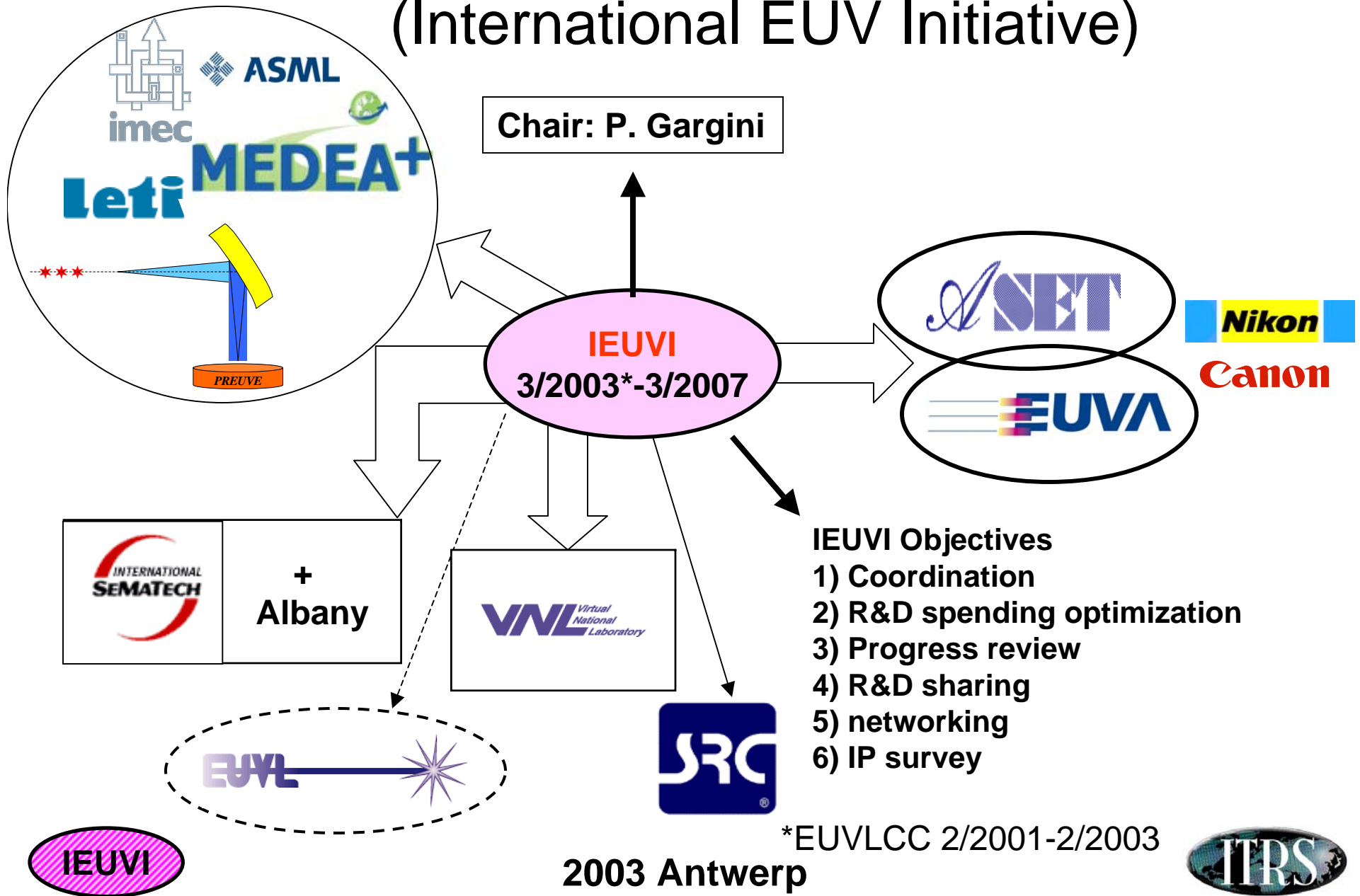


2003 Antwerp



IEUVI

(International EUV Initiative)



Goals of IEUVI

<http://www.ieuvi.org>

1. To coordinate collaboration among world EUVL consortia by:
 - Aligning R&D activities to the International Technology Roadmap for Semiconductors (ITRS)
 - Coordinating R&D collaboration activities among consortia
 - Facilitating dissemination of knowledge of EUVL IP



2003 Antwerp



Goals of IEUVI

<http://www.ieuvi.org>

2. To encourage coordination among suppliers by sharing progress reports
3. To identify implementation issues by:
 - Identifying potential "show stoppers" for EUVL implementation
 - Communicating implementation issues (e.g., to consortia, IC manufacturers, suppliers, and governments)



2003 Antwerp



IEUVI Projects and Accomplishments *

Topic	Status	ASET	LETI	LLC
1. Multi-layer reflectivity round-robin #1	Completed	✓		✓
2. Multi-layer reflectivity round-robin #2	Starting	✓	✓	✓
3. Multi-layer development & characterization		✓	✓	✓
4. Resist LER		✓	✓	✓
5. Sensor		✓		✓
6. Mask blank inspection	In progress			✓
7. Mask modeling	In progress	✓	✓	✓
8. Defect metrology	In progress		✓	✓
9. Optics metrology		✓	✓	
10. Source development			✓	✓

* as of 10/2002, EUVLCC was changed to IEUVI in 2/2003

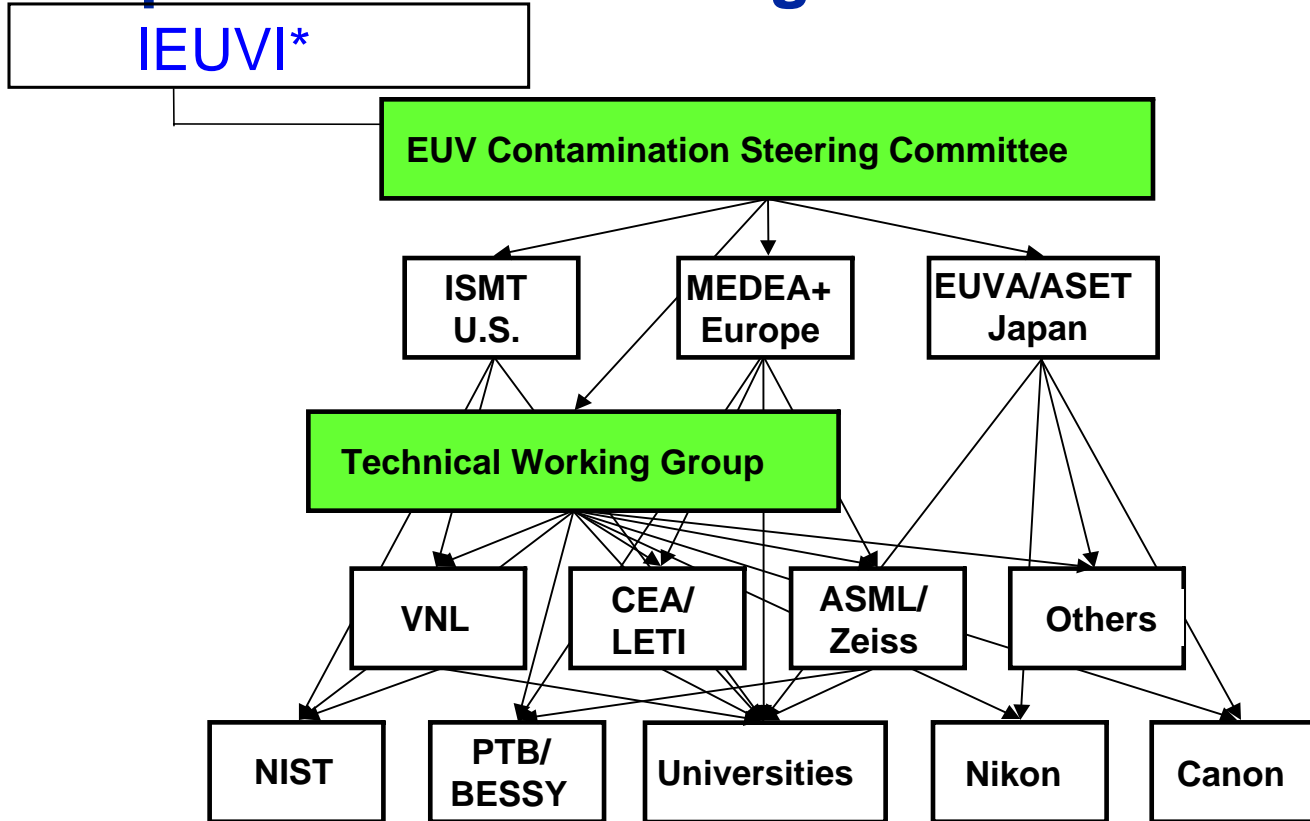


2003 Antwerp



IEUVI Projects

Proposal for Global Organization



 - Proposed

* EUVLCC was changed to IEUVI in 2/2003

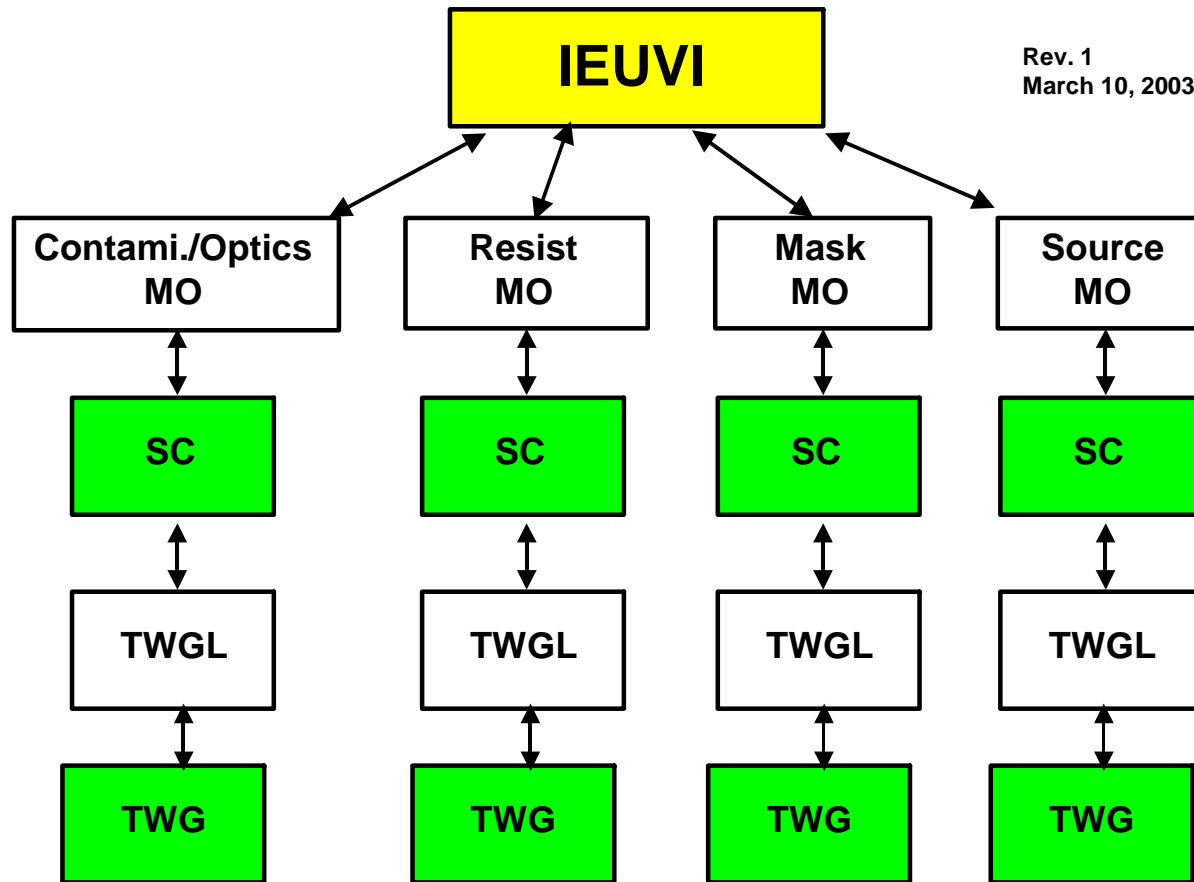
2003 Antwerp

2003/3/11 4時10分
j:\stndpres ¥template ¥IntST.ppt - 18



IEUVI Projects

Rev. 1
March 10, 2003



MO = Meeting Organizer, IEUVI member; SC = Steering Committee
TWGL = Technical Working Group Leader, technical expert; TWG = Technical Working Group



2003 Antwerp



IEUVI Projects

Topic	R&D Entities of Steering Committee	Meeting Organizer (MO)
Contamination/Optics	ASET EUVA MEDEA+ I-SMT	G. Dao of I-SMT
Resist	LETI I-SMT ASET	Brillouet of LETI
Mask	I-SMT ASET MEDEA+	S. Okazaki of ASET
Source	EUVA MEDEA+ I-SMT	A. Ogawa of EUVA, D. Gotz of MEDEA+

- **Collect a list of all international and regional workshops: identify sponsors, objectives, topics, members, dates, meeting frequency etc.**
- **Identify milestones of parallel and of unique approaches**
- **Form a Technical Working Group (TWG), select WG members**
- **MO and TWG members to select a WG Technical Leader (WGTL)**
- **Facilitate TWG, TWG to meet in Antwerp, 2003 IEUVI face-to-face meeting #10**
- **Report status in Antwerp , 2003 IEUVI face-to-face meeting #10**



2003 Antwerp



Highlights of the July 14th IEUVI Meeting

- Discussed EUVL roadmap (e.g., narrowing # of source programs, source power, mask defects, CD control etc.)
- Regional update was given by each Meeting Organizer (MO)
- Reviewed EUVL related conference and workshop schedules to identify opportunities for future TWG meetings
- Resist collaboration among LETI, ISMT, and ASET was presented. Resist TWG to meet on October 2nd.
- A source benchmarking project was proposed by Europe
- Nominated SC's, TWGL's, and TWG members. Members to be finalized during the Antwerp Symposium.
- Discussed regional and global issues associated EUVL source development, funding, and commercialization



2003 Antwerp



THE CHALLENGE: International Collaboration on Extreme Ultraviolet Lithography

- ❖ Europe, Japan and the United States have EUV Lithography Programs
 - Radical departure from current optical lithography, 248 nm, 193 nm, 157nm
 - All reflective optics, 13nm source, multi-layer, atomic precision mask blanks, vacuum operation
 - Required in manufacturing no later than 2009

- ❖ Extreme Ultraviolet = The Prime Candidate for Collaboration

- ❖ **THE CHALLENGE:** Information Exchange Forum (I-EUV-I) is in place under ITRS leadership:
 - Needs your support to move to next phase of cost-shared collaboration
 - WSC should endorse this initiative and sharing of technical risk

WSC 2003 Joint Statement

7. Future Semiconductor Technology Development

The **ITRS** identifies a number of challenges that must be overcome to continue the pace of technology advances, including the introduction of new materials, new lithography technology, and new device structures. **The Members of the WSC unanimously agree that solutions to these challenges are vital to the continued growth and development of the semiconductor industry and that additional resources are needed.** For example, while projects are currently underway in several WSC member geographies to develop **EUV** and other advanced lithography technology to follow after 157nm, the task is beyond the capabilities of any single geography due to the significant cost and complexities involved - **WSC encourages researchers in all regions to further cooperate on this pre-competitive technology.**

European Semiconductor Industry Association (EECA-ESIA)

Japan Electronics and Information Technology Industries Association (JEITA)

Korea Semiconductor Industry Association (KSIA)

Semiconductor Industry Association (SIA)

Taiwan Semiconductor Industry Association (TSIA)

Joint Statement on The Seventh Meeting of World Semiconductor Council (WSC) May 15, 2003, Nice, France



2003 Antwerp



Conclusions

- Functionality of transistors with channel length 5-6nm and has been demonstrated (VLSI Symposium)
- 300mm transition resets the cost/unit area back to 10 years ago
- Revolutionary technologies require funding to success for ~20 years
 - No single consortium, organization or country can support the whole bill
- IEUVI provides a forum for international cooperation towards commercialization of EUV in 2009
- The need to explore ways for cost sharing among different regions has been endorsed by the WSC 2003 meeting



2003 Antwerp

