SEMATECH EUV Mask Workshop
Miyazaki, Japan NOVEMBER 1, 2004

Wafer FAB and Mask Manufacture Strategy - when does the mask go bad ? Breakout Session #2 Results

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Acknowledge: Jan Hendrik Peters

Proposed questions for discussion in Breakout Session #2

- Two scenario's were discussed in detail
  - Continue with current model of IC FAB sending masks back to Mask house for cleaning, repair, carriers
  - Clean, repair, and inspect masks at the IC FAB.

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Breakout session #2 : EUV Mask & wafer FAB Strategy:

- Group consensus was that IC FAB and mask house should continue the current model of shipping dirty masks back to M.H. for servicing.
- Issues with IC FAB taking responsibility of inspection, cleaning, etc.
  - Mask inspection tools are expensive and will add costs to FAB operation and wafer CoO
  - Current cleaning technology / know-how usually proprietary within the mask shop. Unsure if the required newer I.C. FAB cleaning procedures for EUV masks would be transferred to FAB's or licensed by Mask Houses.
  - Potential of different cleaning technology / process for each mask supplier (i.e. different absorber materials, capping, etc.)

Breakout session #2 : EUV Mask & wafer FAB Strategy:

- Issues with IC FAB taking responsibility of inspection, cleaning, etc. (continued)
  - How often will masks need to be cleaned ? Can Sematech conduct a study to support this ?
  - How does damage caused by aggressive cleaning impact IC FAB cleaning
    - Cleaning of defects can be verified through inspection (optical or @ λ)
    - Molecular contamination bigger concern – manifest / increase impact over time (first inspection may not identify molecular contamination)
- Continue with current process of IC FAB sending masks back to M.H. (Issues)
  - Stable cleaning processes are required to support removal of particle defects. Cost to service by M.H. is cleaning and defect inspection
  - However damage to mask by cleaning may impact CD performance and cost more (cleaning, defect inspection, CD inspection w/ statistics)

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Breakout session #2 : EUV Mask & wafer FAB Strategy:

- Will all defects cause killer device (yield hits) ? Strategy of allowing IC FAB and M.H. to agree on known defects in mask.
  - Defects that do print but do not cause electrical performance issue at die
  - M.H. can send “defect maps” of the starting blank to I.C. FAB so IC FAB and device layout team can assess if defect locations are o.k.
  - Good standardization needed for defect fiducial marking
- Mask House will require the same carriers that are used in the I.C. FAB to be used to ship EUV masks to and from M.H. / IC FAB
  - The inner protective pod needs to be compatible with M.H tooling
  - Shipping must include the double pod

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