Challenges for the Integrated Manufacturing of EUV Masks

Christian Holfeld, Uwe Dersch, Anna Tchikoulaeva, Eric Cotte, Christian Chovino, Jan Hendrik Peters

Advanced Mask Technology Center, Dresden, Germany

Florian Letzkus, Jörg Butschke, Corinna Koepernik

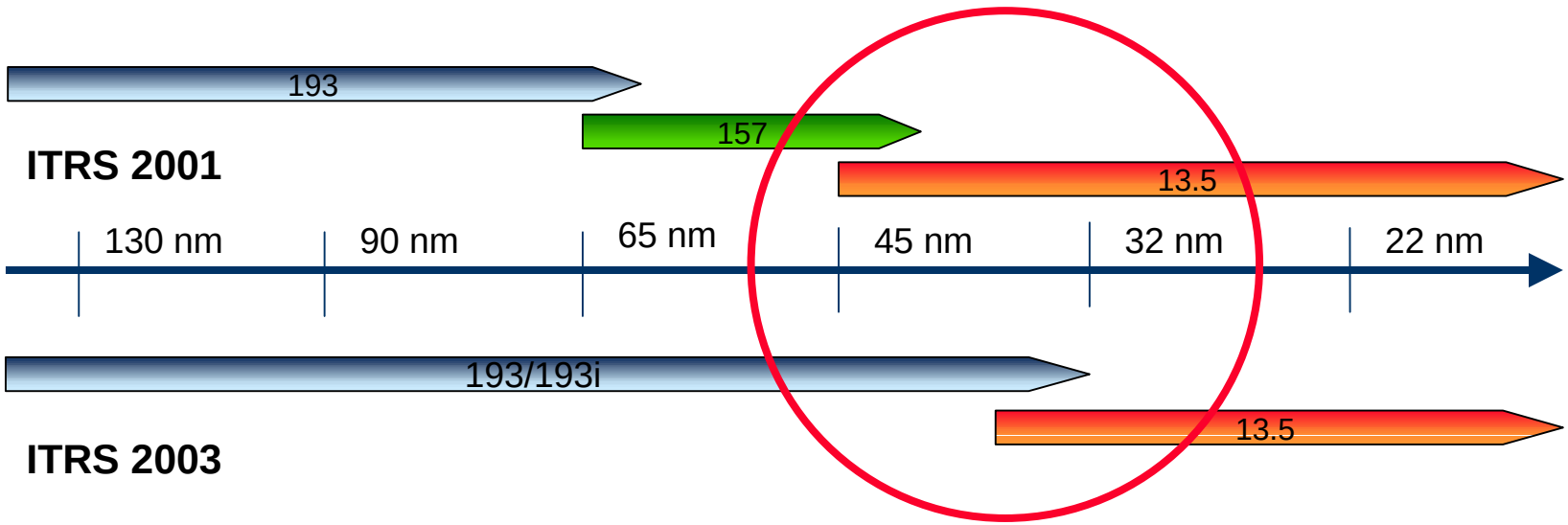
IMS-Chips, Stuttgart, Germany

3rd International EUVL Symposium, Miyazaki (Japan), 2004

Outline

- Introduction
- Integration of mask processes
- Mask manufacturing
- Mask printing
- Conclusion

Industry Roadmap



Integration of Process Steps

Previously, the process feasibility of EUV masks has been shown.

But: How to establish a consistent mask manufacturing?

Process integration →

- complete run of process flow
- definition of mask specifications
- full-field mask performance
- defect-free handling

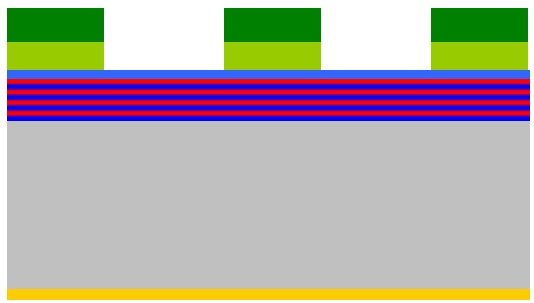
Goal: Deliver qualified masks for successful EUV printing.

Basic Process Flow for EUV Masks

Commercial mask blank

Mask fabrication

- Resist coating
- Pattern generation
- Resist development
- Absorber etch
- Resist strip
- Defect inspection
- Repair
- Buffer etch
- Clean



EUV printing mask

3rd International EUVL Symposium, Miyazaki (Japan), 2004

Basic Process Flow for EUV Masks

Mask fabrication

Commercial mask blank

- Resist coating
- Pattern generation
- Resist development
- Absorber etch
- Resist strip
- Defect inspection
- Repair
- Buffer etch
- Clean

EUV printing mask

Mask metrology

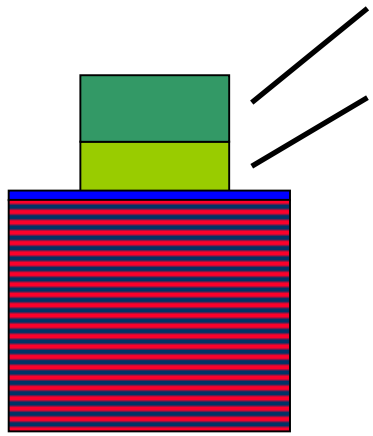
- CD
- CD linearity
- CD uniformity
- LER
- Registration
- EUV reflectance
- Side-wall angle

…

EUV Mask Stack

Criteria for mask materials:

- EUV contrast
- absorber stack thickness
- etch selectivity
- etch bias
- repair process
- environmental stability



✓ high EUV contrast (measured 99.4%)
✓ low etch bias
✓ ML protection during repair

Challenges for the Integrated Mask Manufacturing

Key issues

- repair of defects
- defect and CD metrology
- printing performance of mask

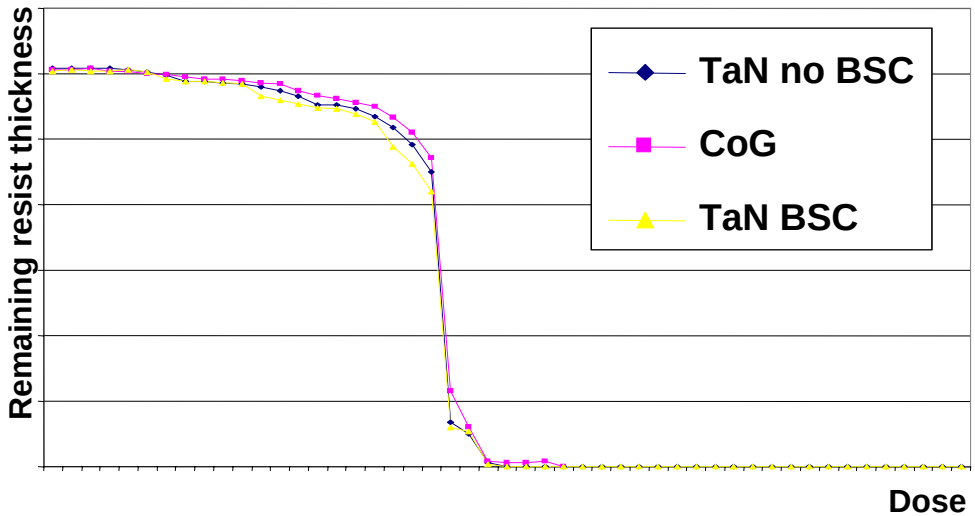
Improvement of standard mask processes

- influence of backside coating
- simultaneous patterning of different feature type and sizes
- uniformity of processes

Backside Coating

Does the backside coating influence the resist patterning?

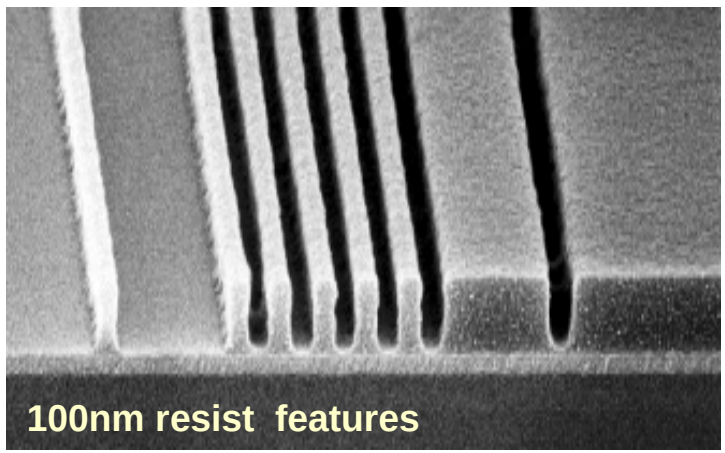
→ dose-to-clear experiment for resist process



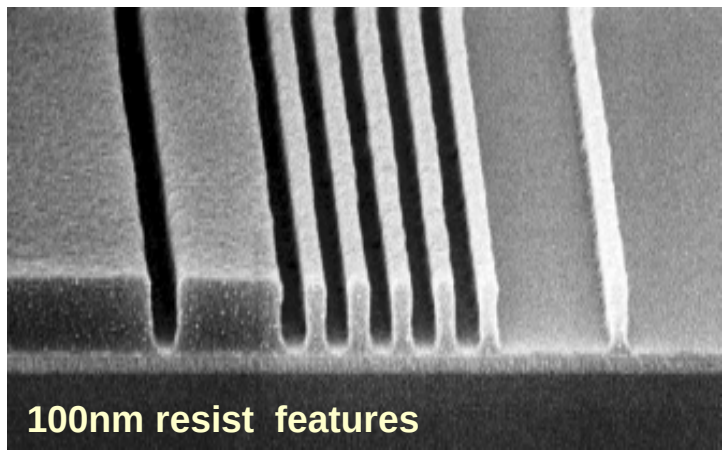
→ No difference in resist contrast by e-beam writing
→ Backside coating does not influence the resist process

Backside Coating

Does the backside coating influence the resist patterning?



Blank without BS coating

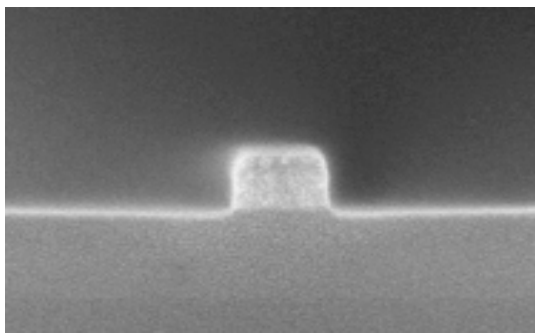


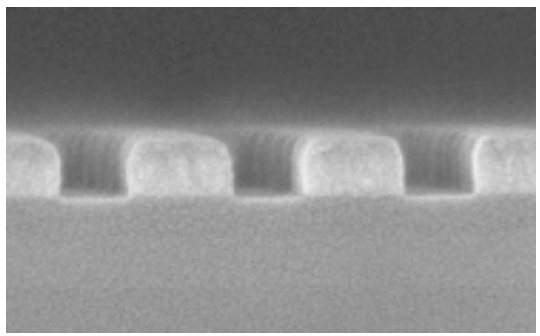
Blank with BS coating

→ Resist profiles remain unchanged

EUV Mask Patterning

absorber etch

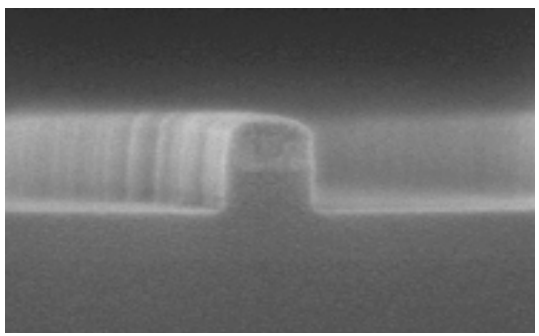


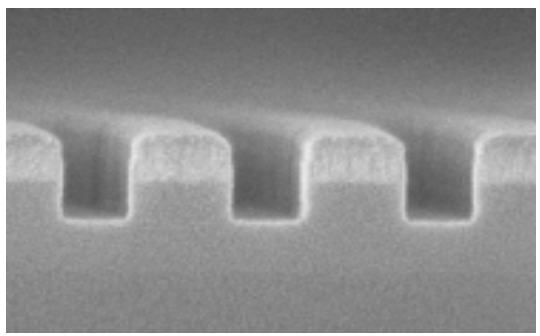


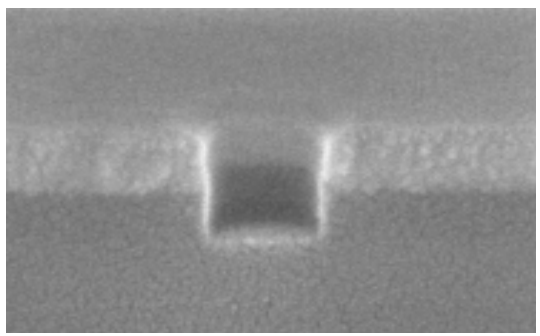
125-nm features on mask

(corresponding approx.
32-nm features on wafer)

buffer etch







Isolated line

Dense line

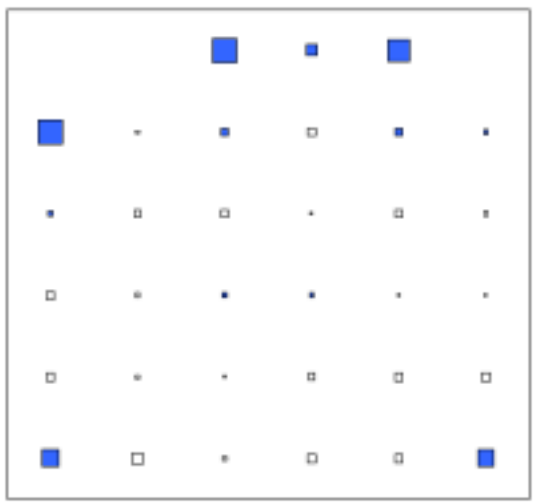
Contact hole

→ Mask pattern resolution of EUV target nodes
→ Good sidewalls angles, no undercut

EUV Mask Patterning

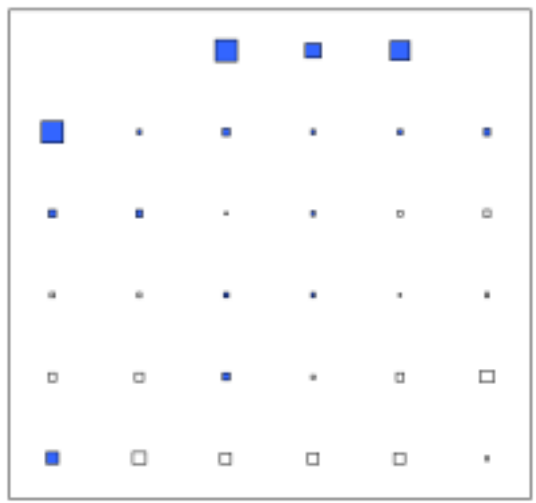
CD Uniformity for 150-nm dense lines

after absorber etch

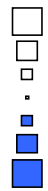


CDU = 11.9 nm (3σ)

after buffer etch

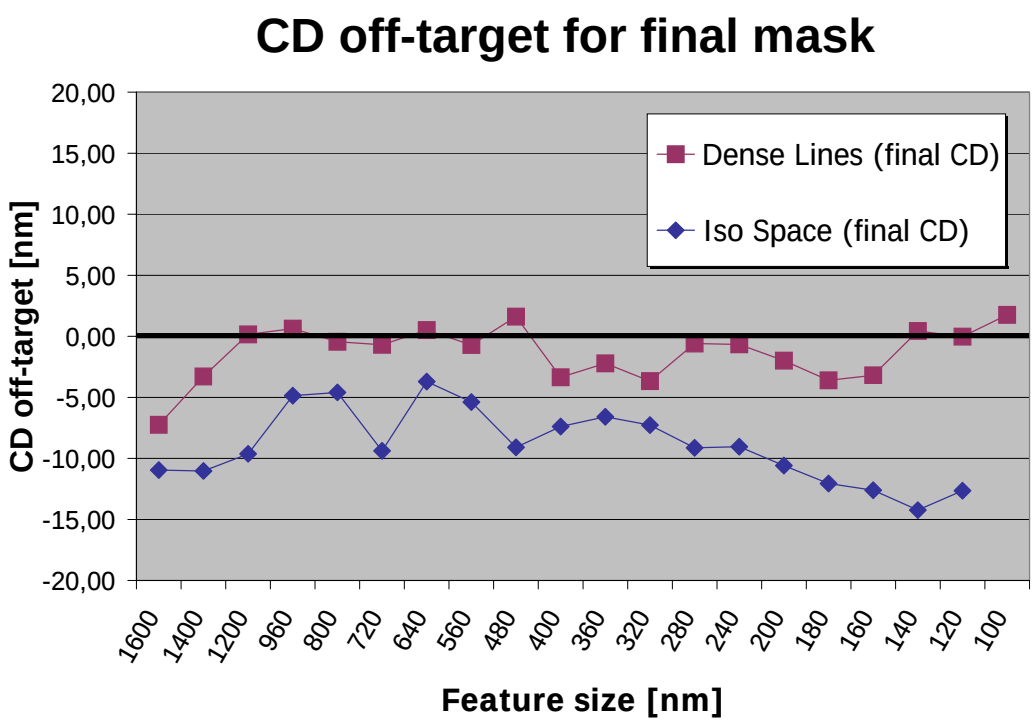


CDU = 11.1 nm (3σ)



→ CD uniformity maintained during buffer etch
→ Performance of integrated process needs further improvement
→ Latest results: CDU ~ 7nm

EUV Mask Patterning

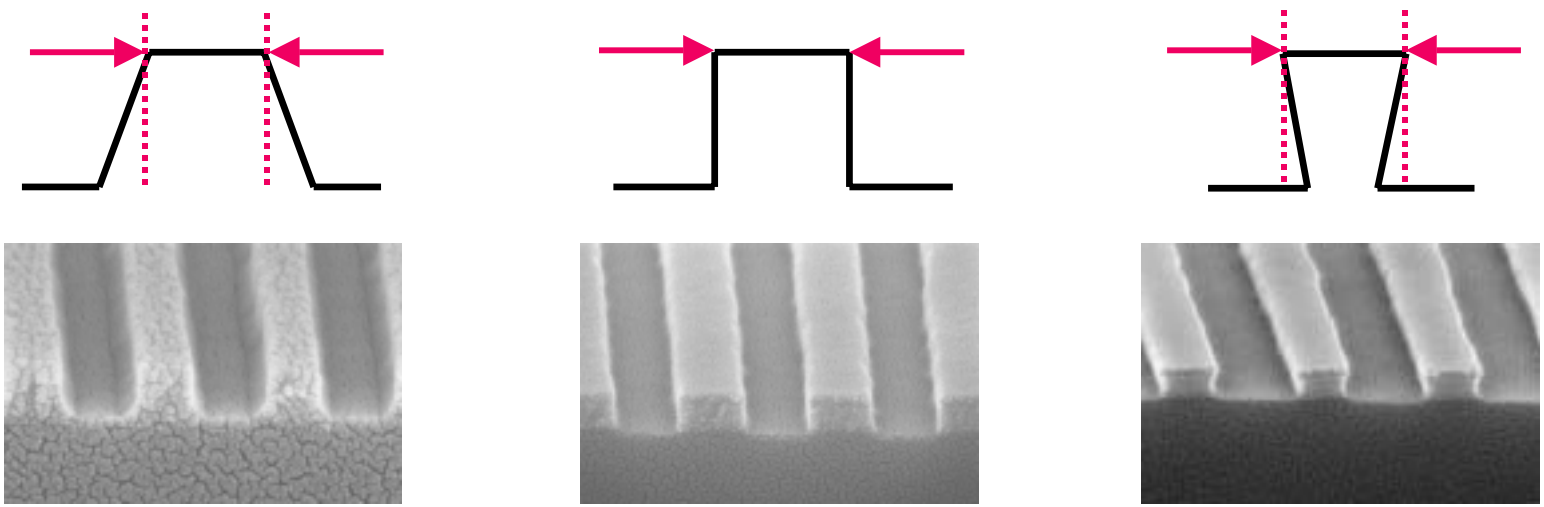


→ Good linearity down to 100nm mask features

→ Non-optimized proximity correction for e-beam writing

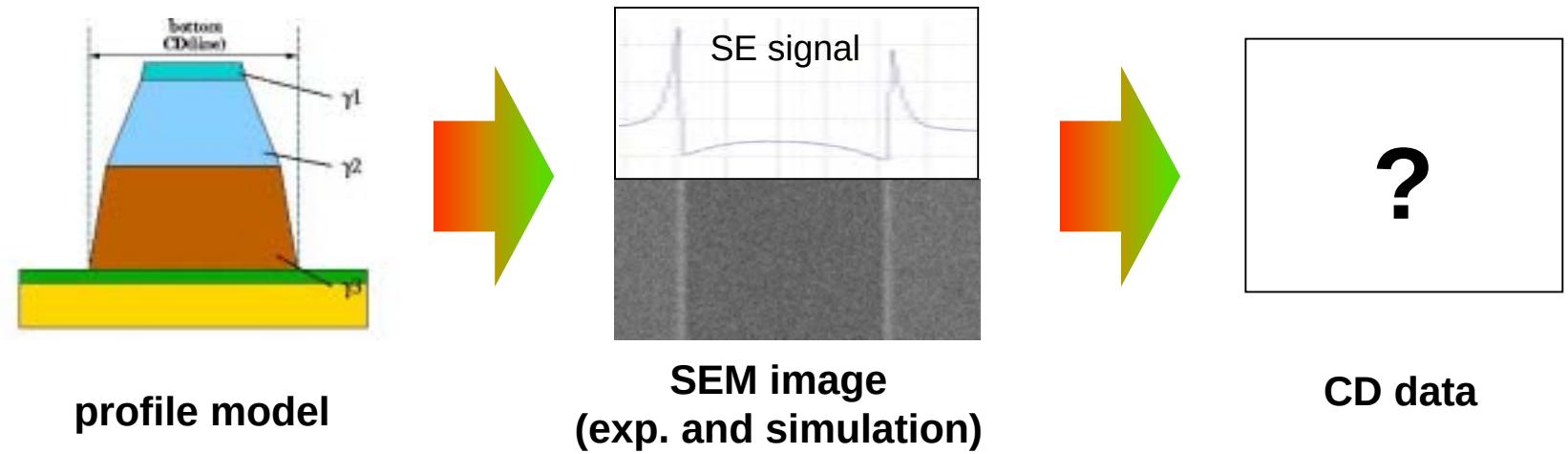
Impact of Line Profile to CD Metrology

- How does the measured signal relate to the geometrical profile?
- What feature of the line profile is measured?
- How is the line profile related to light modulation during exposure?



Impact of Line Profile to CD Metrology

Approach:
- Simulate SEM signal for model profiles
- Compare with real measurements
- Understand impact of 3D topography



profile model

SEM image (exp. and simulation)

CD data

→ Work ongoing to improve CD metrology

Defect-free Mask Manufacturing

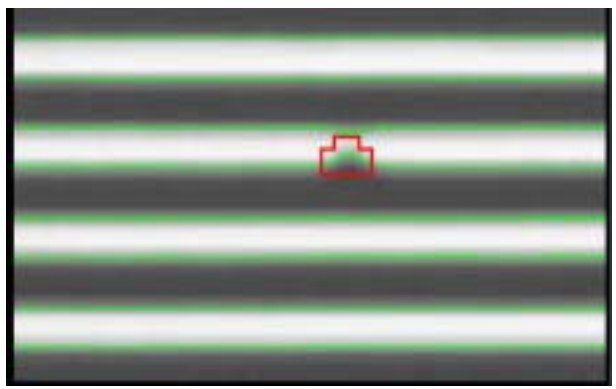
- Defect-free blanks and reticles are most critical showstopper for the EUV technology
- Critical defect size dramatically decreases → huge challenge for manufacturing and metrology

- Strategy:
  - –defect reduction from mask handling
  - –defect detection on mask
  - –damage-free repair capability

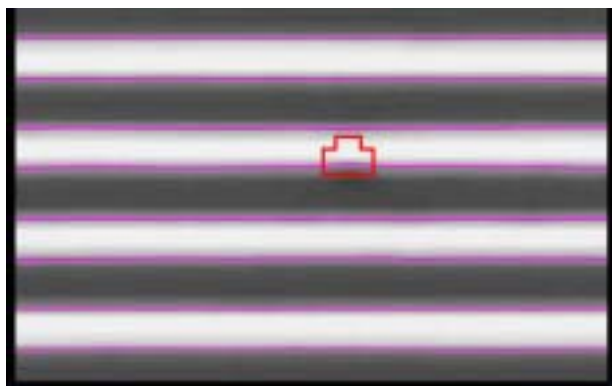
Defect Inspection

- Automatic pattern inspection (die-to-die)
- 257nm inspection wavelength, reflection mode, 125nm pixel size

Die 1: Programmed defect
(180nm extension, 450nm DL)



Die 2: Repaired defect
(same site as in first die)

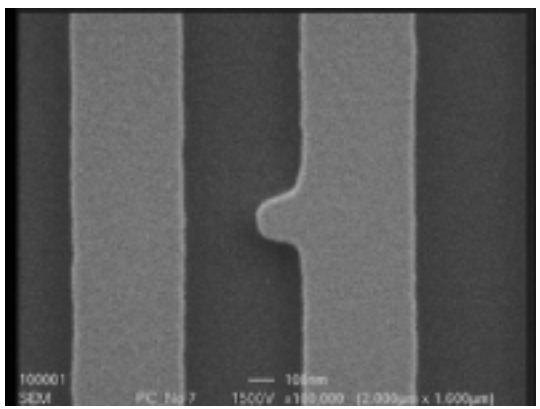


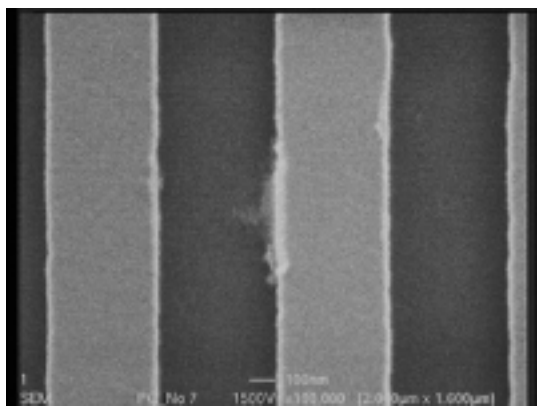
→ Pattern differences can be found automatically

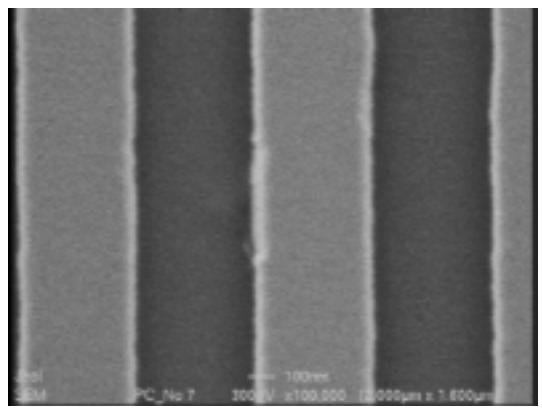
Nanomachining of Defects

- Repair process is essential for mask manufacturing!

Programmed defect → **Removal with RAVE** → **After buffer etch**





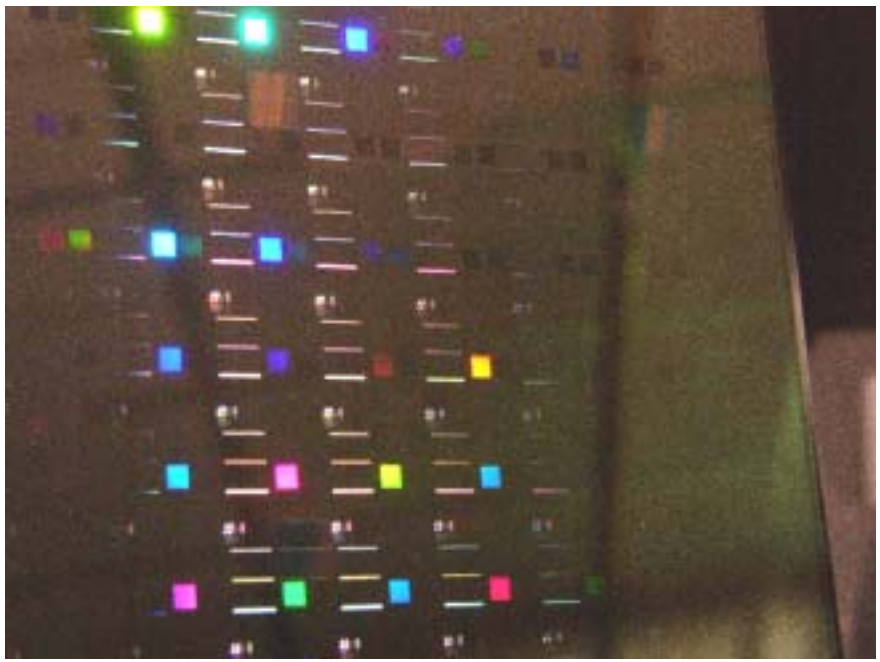


(180nm dark extension)

See also our poster MaP12!

→ Successful repair of programmed defects; various sizes done

Full EUV absorber mask



- full mask process flow established
- mask performance qualified with printing test at the MET tool

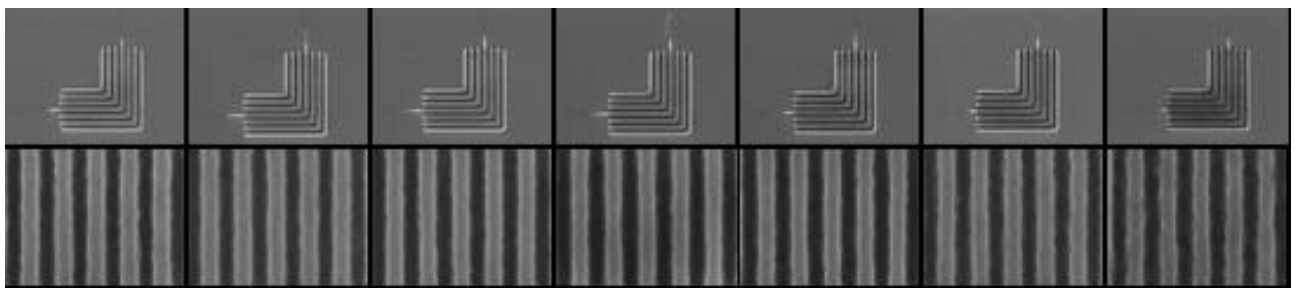
EUV Printing Performance

Example:

60nm elbow/dense lines (wafer size), 5x demagnification

printing on MET at LBNL in cooperation with AMD and Infineon

through focus at best dose



–150 nm 0 nm +150 nm

(BACUS 2004, 5567-82)

→ Good printing performance under various conditions

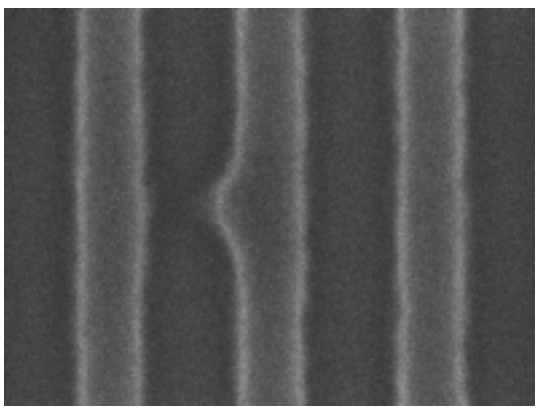
Repair Verification

Example:

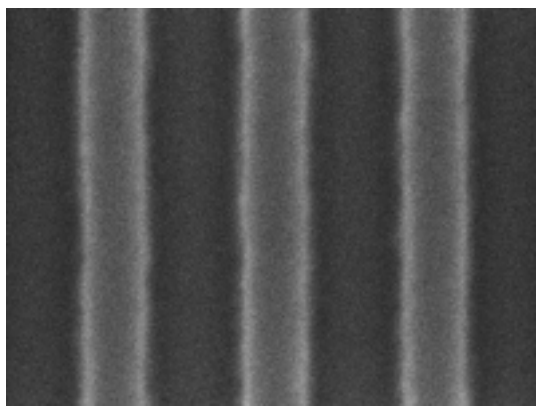
Programmed defect: 45nm dark extension, 90nm dense lines (wafer size)

Printing of repaired site and of reference defect

Reference defect



Repaired defect



→ Damage-free repair capability

Summary

- Complete process flow for EUV absorber masks has been established
- Processes targeted to sub-50nm nodes
- Resolution of 125nm features achieved on mask
  (isolated lines, dense lines, contact holes)
- Damage-free repair process available
- Successful EUV printing of manufactured masks

Acknowledgments

The AMTC gratefully acknowledges the financial support

- by the German Federal Ministry of Education and Research (BMBF) under Contract No. 01M3154A (“Abbildungsmethodiken für nanoelektronische Bauelemente”)

and

- by the European Commission under Contract No. 507754 (More Moore)