TECHNOLOGY CENTER

SEMI PIC EUV Working Group Meeting

# “Warm up”

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# *EUVL facts*

lithography technology for 3x nm node and smaller

- 13.5 nm wavelength, 4:1 diminution mask to wafer pattern
- Multi “level” mask
- No pellicle protection during exposure

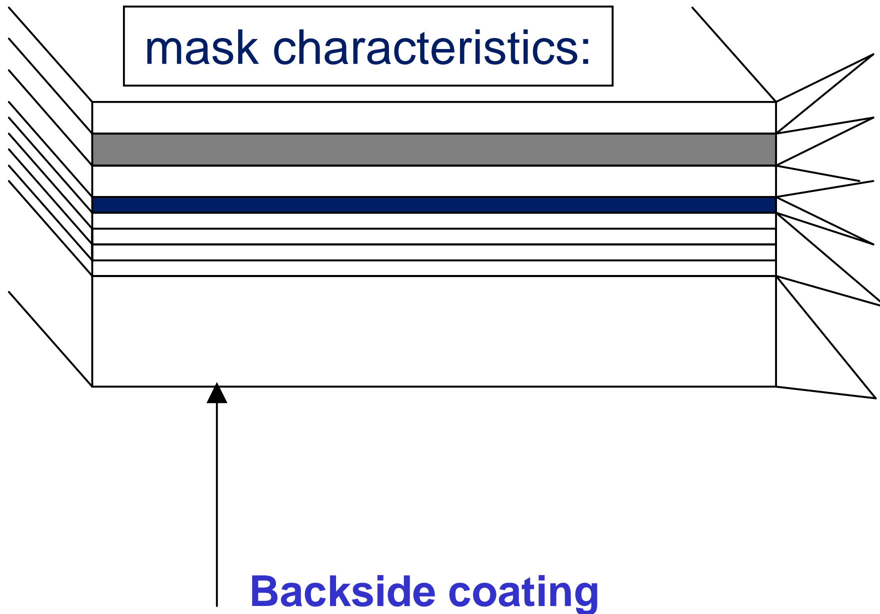
ITRS Particle Spec < 5 “23nm” @patterned side

- Reflecting/absorbing light patterned masks exposure (No transmission light exposure)
- Exposure via mirrors instead of lenses
- High vacuum process

Molecular Contamination Spec e.g. AMC, ion residues, metals, organics & water

- Highest Utilization required

Throughput, evolutionally Fab integration




**Resist**

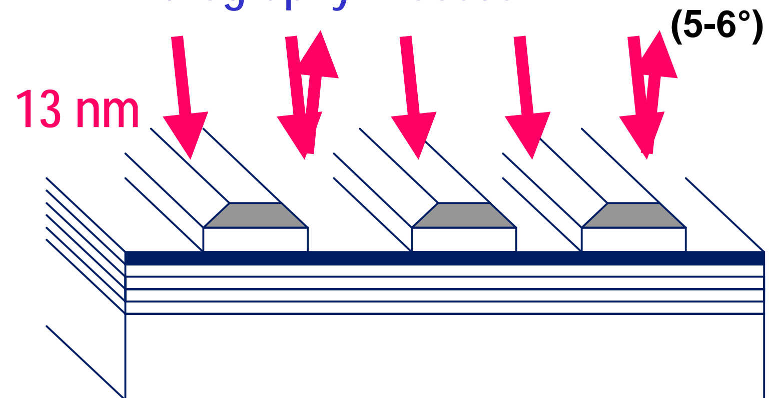
**Absorber, defines dark features**

**Buffer (protects multilayer)**

**Capping Layer (seals multilayer)**

**Multilayer, reflects EUV light**

**Low thermal expansion substrate**



**Performance requirements**

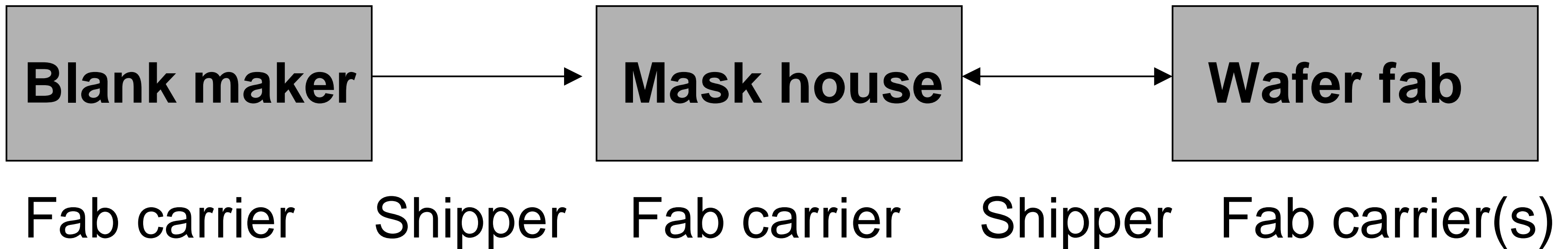
- **ITRS Particle Spec “23nm”@patterned side**
- **Molecular Contamination Spec**
  **(e.g. AMC, ion residues, metals, organics & water)**
- **Throughput, evolutionally Fab integration**

Do we / should we include
basic performance requirements to PIC SEMI Standard(s)

or should
SEMI Micropatterning TF create Standard
and/or
SEMATECH give Guidelines (best practise)

Who will compile the specs

**3** PIC end users:




Fab carrier Shipper Fab carrier Shipper Fab carrier(s)

?

- one carriers design for all
- one design concept tailored for specific applications
- Applications optimized carrier designs

&

Corresponding physical interfaces

Blank inspection

Data preparation

Resist coating

Pattern generation

Litho process

Etch

Clean

Metrology

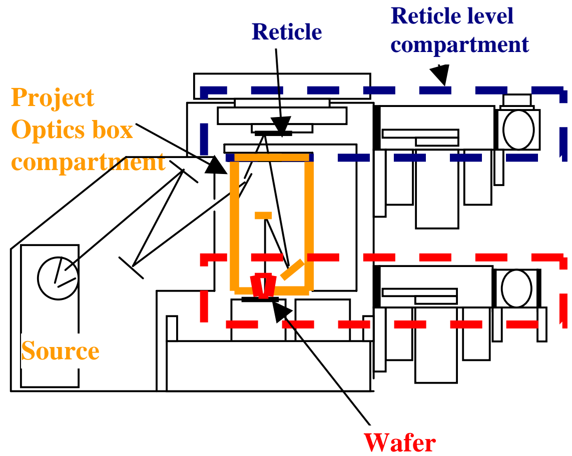
IF Multilevel mask

Inspection

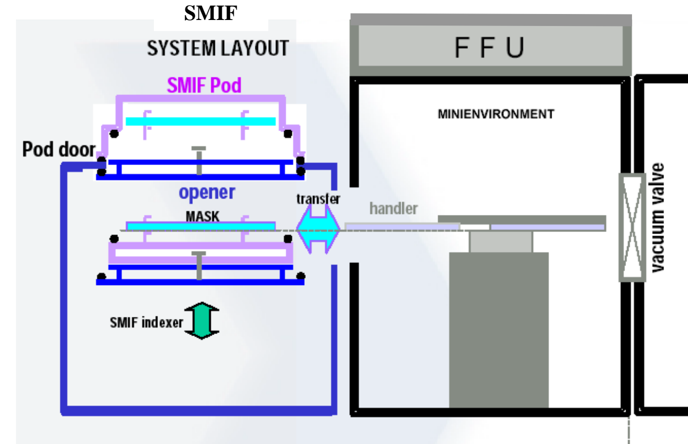
IF Repair

Final clean

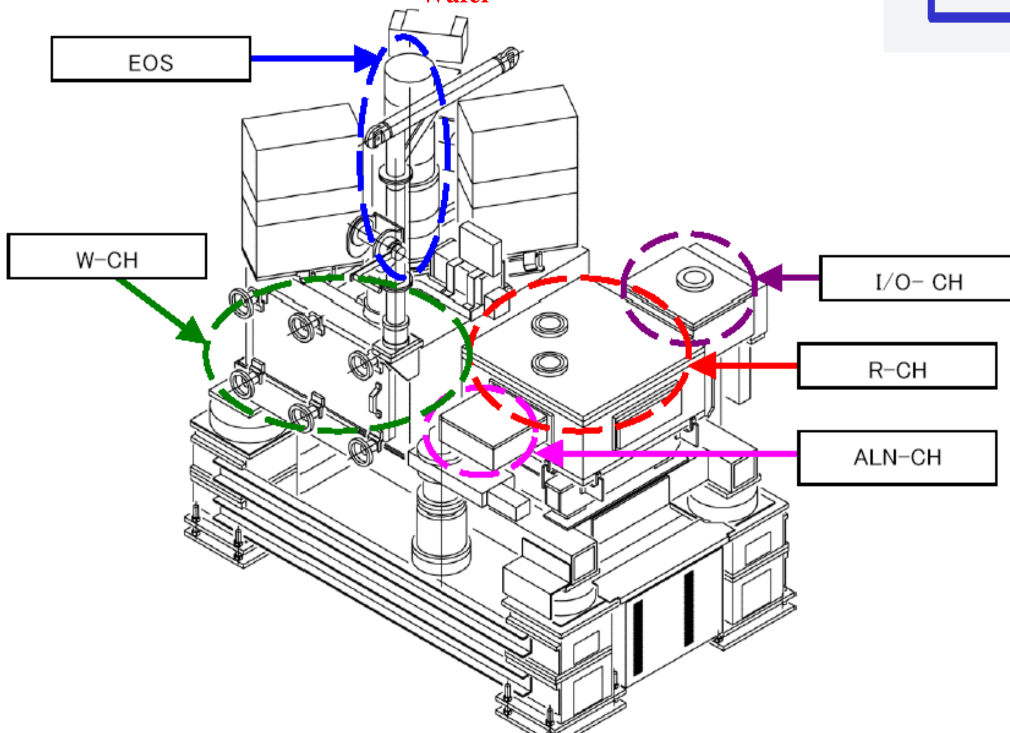
**Black box MASK HOUSE**



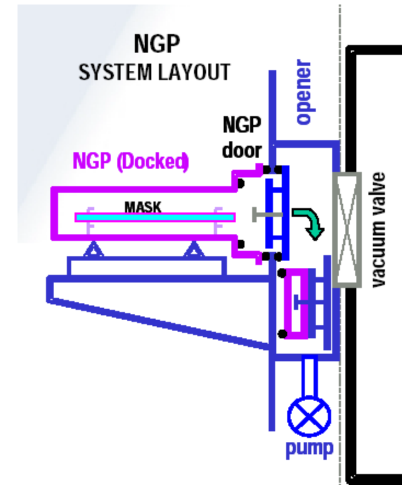
Reticle
Reticle level compartment
Project Optics box compartment
Source
Wafer

SMIF
SYSTEM LAYOUT
F F U
SMIF Pod
MINIENVIRONMENT
Pod door
opener
transfer
handler
MASK
vacuum valve
SMIF indexer

EOS
W-CH
I/O- CH
R-CH
ALN-CH

NGP
SYSTEM LAYOUT
opener
NGP door
NGP (Docked)
MASK
vacuum valve
pump