Technique for determining a prudent voltage stress to improve product quality & reliability

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Prudent Voltage Stressing

Environmental

- Continually decreasing time to market
- Temperature & voltage stressing are both traditional, but …
- Misapplication (overstress) can produce artifacts and defects, & conversely …
- Understress permits defects to escape screening, at great cost to manufacturer and customer alike

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Traditional Approach

- Split lot experiments
  - Stressed product vs unstressed control
    - ∆ If sample size too small, get null result
      - If stress too mild, get null result
      - If stress too severe, defect-free product is degraded
- How can one predict sample size & stress severity economically & effectively?

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Sample Size Algorithm

- Sample size is established by control group failure rate + Fisher's Exact Test
  - Say control group fails at 1% & you want a measurable reduction …
  - If your stress is effective enough to produce zero failure rate (kills all defects), Do you want 1/100 vs 0/100 or 3/300 vs 0/300 or 10/1000 vs 0/1000?
  - If you pick a 90% confidence level, sample size of 300 per split is sufficient (not shown here or paper)

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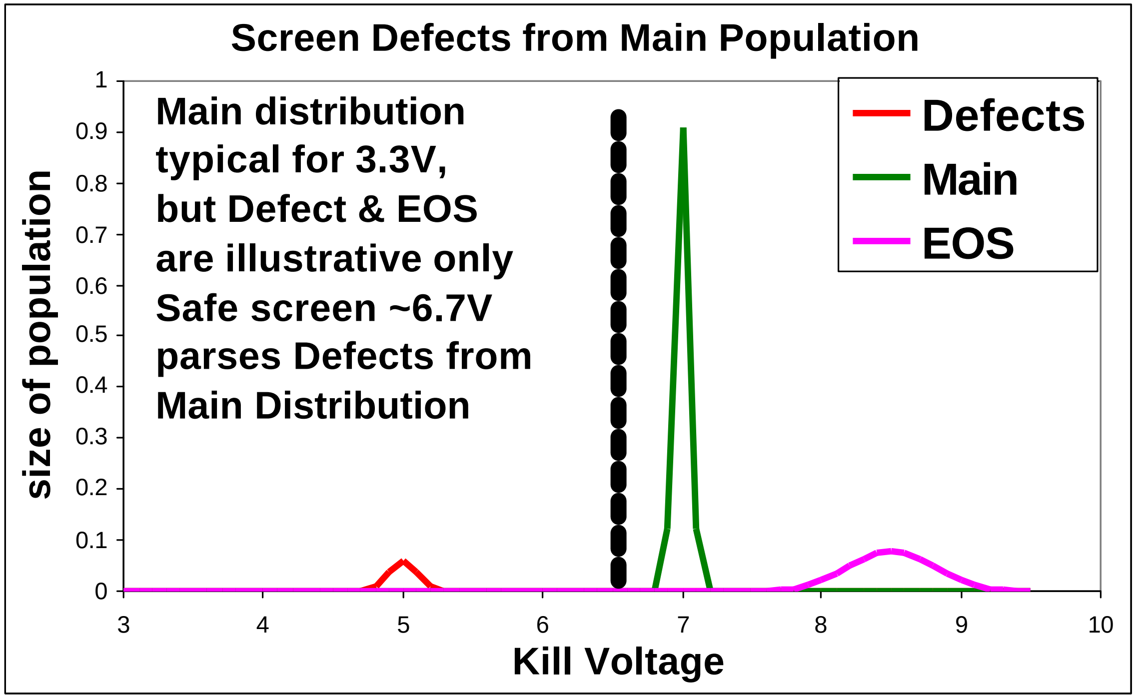
Qualitative view of Product Screen

- What if product kill voltage disti were bimodal?
  - Some defective product fails much earlier



- Prudently chosen screen (dotted line) separates defective product from main population

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Prudent Voltage Stress Assumptions

- Assume we have 2 populations
  - A small, screenable defect-laden population
    - Δ Small sample size will not have ANY defects
  - A large defect-free population
    - Δ Expect Gaussian voltage to kill
- Killing stress for **both** populations increases **exponentially** with voltage, but **much** faster for defective product ... basis for the screen

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Killing Voltage on Small Samples

- Small samples will be defect free
- Kill voltage should be Gaussian (weakest element to fail), but …
- Some stresses will produce multiple modes
  - If stress duration is too long, then excessive temperature produces a second mode with large σ
    - σ is the dispersion in kill voltage
    - Suggest stress duration of 10 - 300 msec
  - Some product won't fail (reason N/A), but we need only to characterize the most sensitive tail

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Incremental Approach for Kill Voltage

- Since stress varies exponentially with voltage, small voltage increments (interspersed with parametric & functional test at datasheet) until failure will ultimately establish kill voltage
  - Nominal gate oxide electric field is ~5 MV/cm & intrinsic slope is ~ 1 decade per MV/cm, so 6% more V_{cc} doubles stress for defect-free material (perhaps 2% in V_{cc} will double stress for defects)
  - We find V_{cc} increments of ~3%/step effective
  - If you find σ ~ 50-100 mV (normal probability plot), then you have successfully found the kill voltage

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Kill Voltage - Tips & Implications

- Plot data as normal probability to establish # of modes
  - If multiple modes, parse the data to get good estimate of kill voltage & σ for lowest mode
  - If lowest mode has large σ, then consider reduced duration or temperature or better heat sink, etc.
- Some damage will have been done prior to final kill, but the damage from preceding stresses will vary something like ...
  - 1, $1/\sqrt{2}$, 1/2, $1/2\sqrt{2}$, 1/4, $1/4\sqrt{2}$, 1/8, etc.
  - Proper screen will be ~ 2 steps smaller than kill V

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Kill Voltage in Practice

- Damage series suggests screen ~2 steps<kill, other factors introduce much more uncertainty
  - within lot variance or lot to lot variance
  - long extrapolation from mean V_{kill} to V_{safe}
    - Δ Small sample size means we have data from -1 to +1 σ, but we define V_{safe} screen as V_{kill} - 6σ, as 6σ corresponds to only a ppb damage to the defect-free population
  - Clearly prudent to pick screen based on smallest V_{safe}, else damage some of the defect-free product

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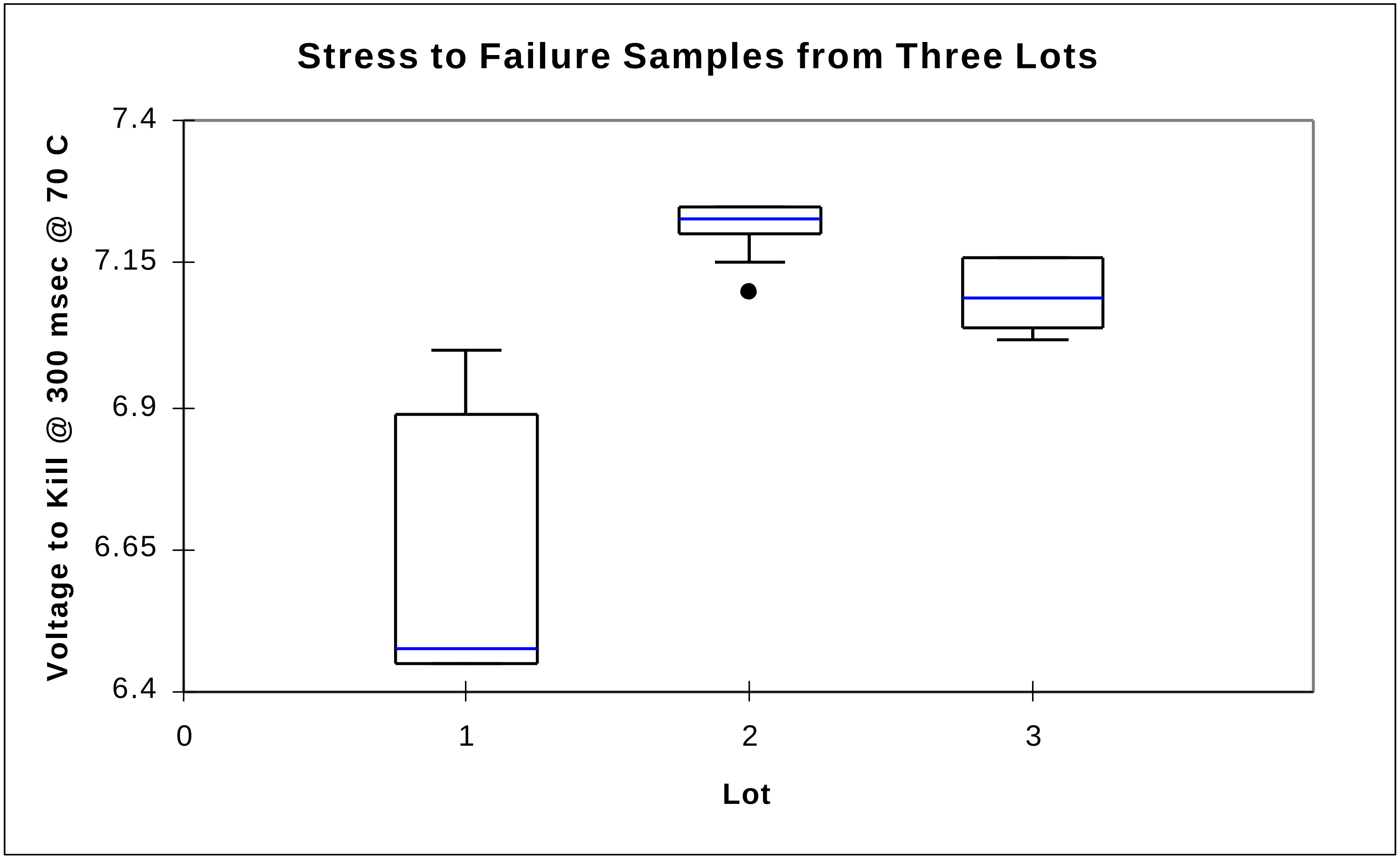
Practical Illustration (LAN product)

- V_{kill} for Lot 1 << Lots 2 & 3 (box/whisker plot)



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Practical Illustration (cont.)

- V_{kill} for 4th & 5th lots consistent w/ 2nd & 3rd
  - Cause Not Found for low value in 1st lot

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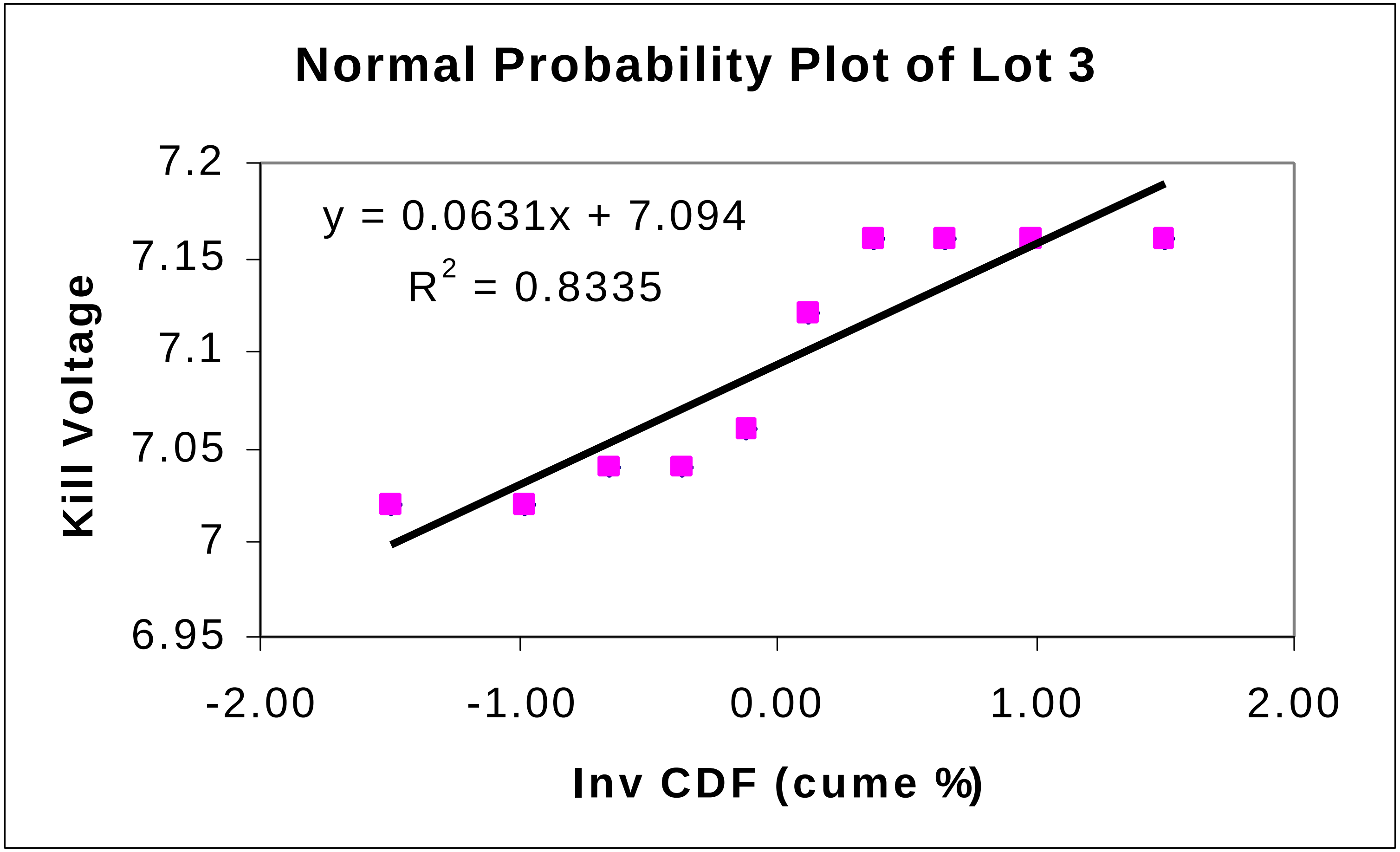
Normal Probability Plot for V_{kill}

- Note small σ & large mean V_{kill} (>2*nominal)



 R Blish et al Oct 2000

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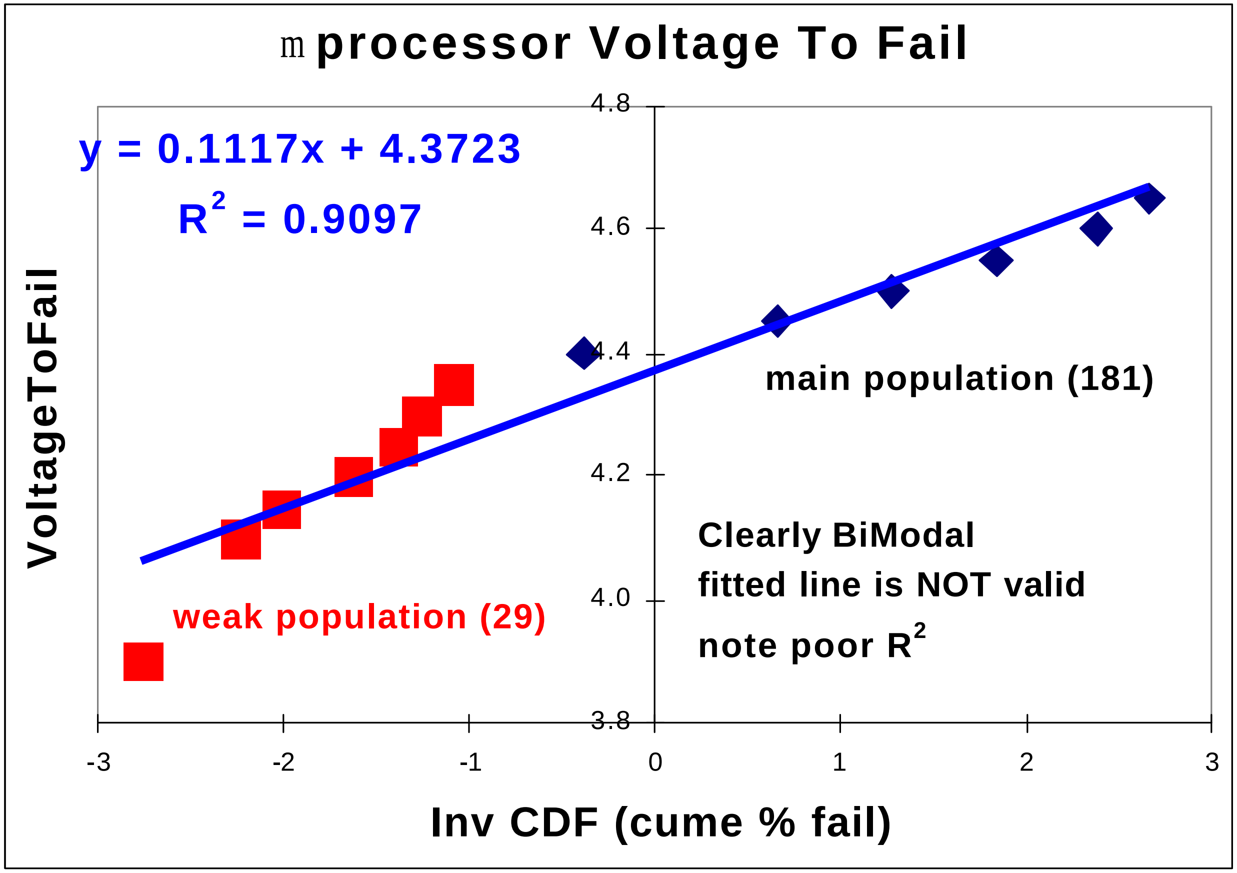
2nd Practical Illustration - microprocessor

- Early eng. runs had a weak population
  - Don't extract mean & σ from single plot if bimodal



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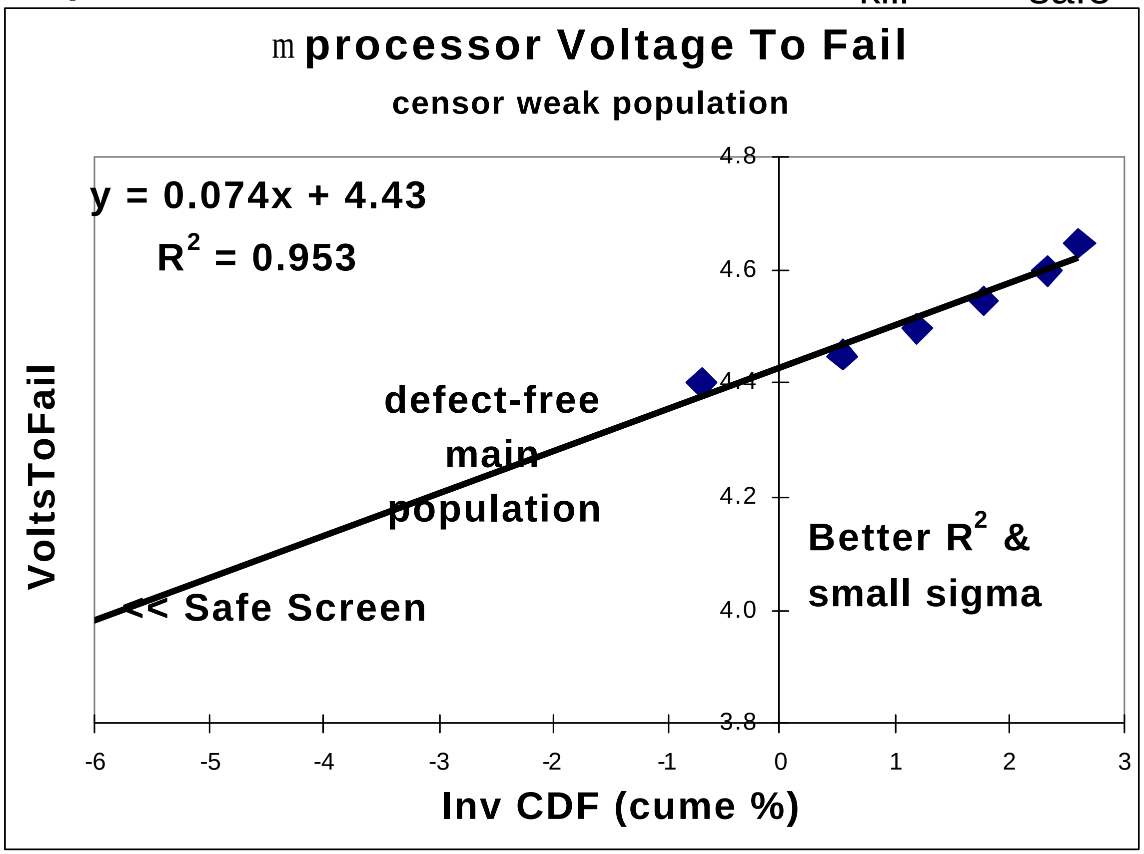
Parse mpr data - only main pop. shown

- σ only 74 mV & mean V_{kill} 130% * nominal
  - V_{safe} at -6σ ~4.0V, ~ 120% * nominal V_{cc}
  - Better process increased ratio of V_{kill} & V_{safe} to nominal



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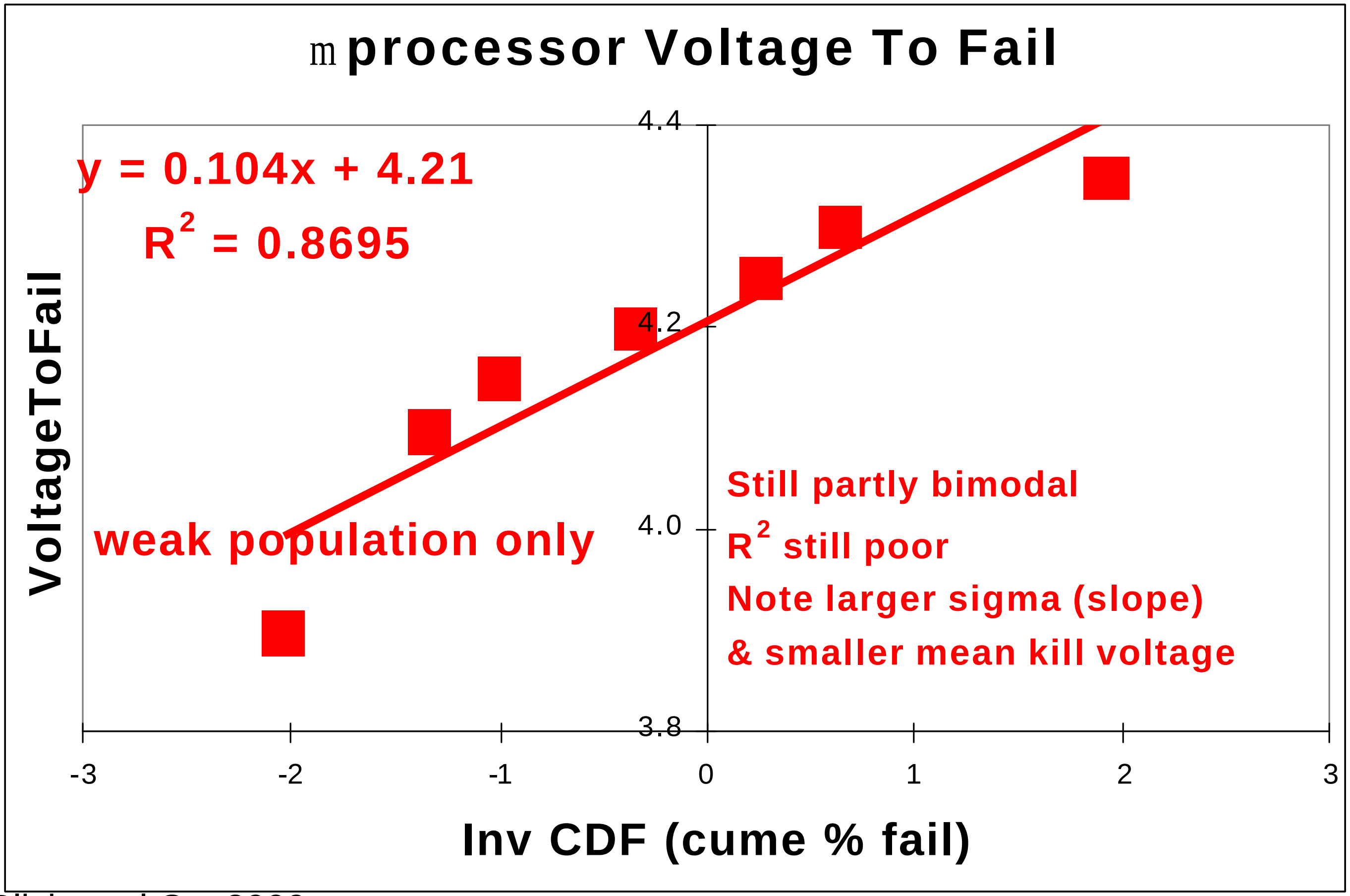
Normal probability plot for μpr weak pop.

- Smaller V_{kill} and larger σ than main pop.



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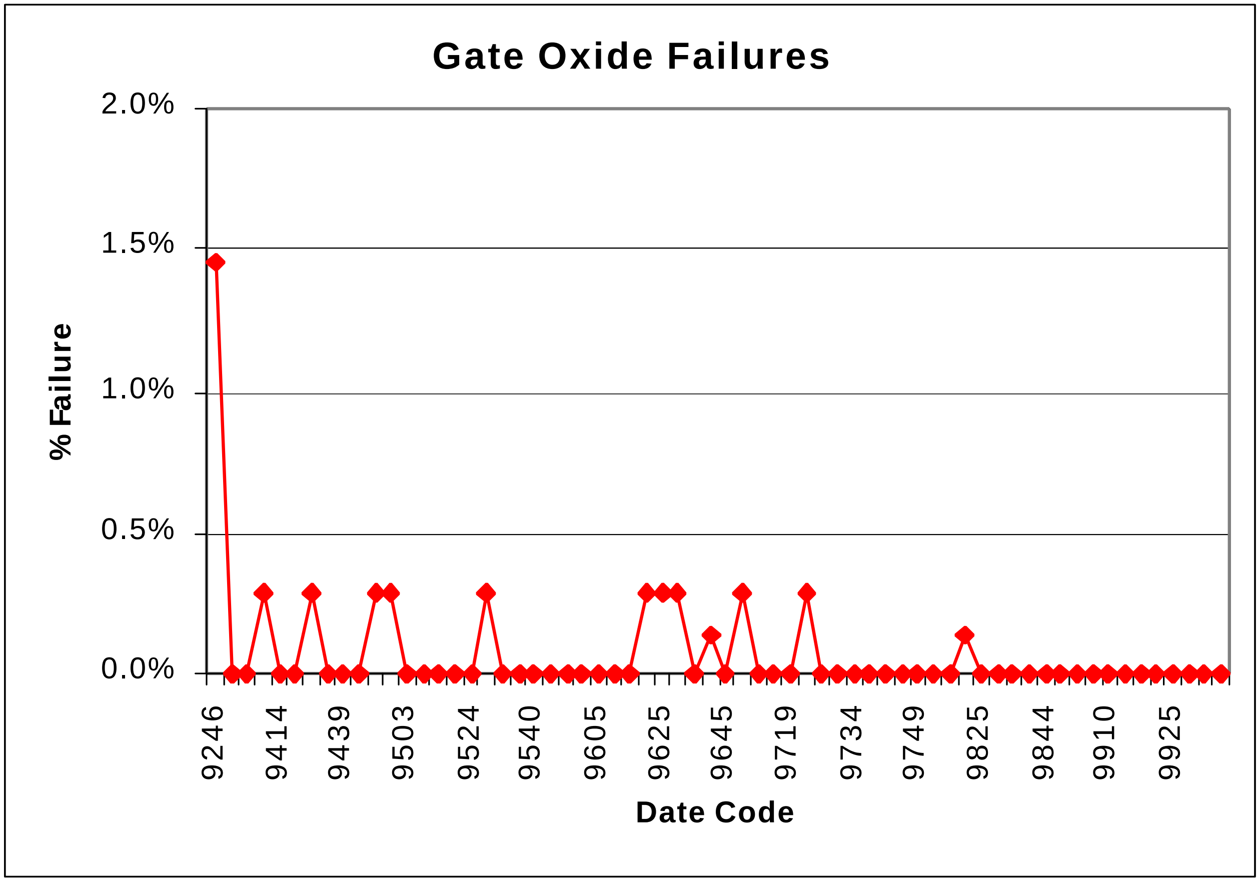
Payoff - Reliability Monitor (7 yr)

- Gate ox problem finally fixed w/ screen in '97
  - Screen at class easier than fixing ancient process



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Issues for future work

- Need more efficient way to refine σ estimate
  - Imprecise σ estimate has strong effect on V_{safe}
- Need better way to pick stress duration & node coverage (dynamic or static)
- Need to understand sources of variance
  - Probably need ANOVA & DOE (factorial expts.)
  - Why are some devices “immune” to voltage stress?
- Need to move from “dead body count” to FA basis
  - If parse multimodal data, know exactly which sample(s) are most representative (central) to own mode(s)
- Need V_{safe} vs temperature (SWAG now)

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Summary

- Voltage stress is effective screen, if prudent
- Simple procedure is used to determine V_{safe}
  - Based on incremental voltage stress, Gaussian V_{kill} & extrapolation to -6σ for V_{safe}
  - V_{safe} kills defects, but leaves main pop. unharmed
  - Best screens are <0.3 sec to prevent overheating
- Applied to wide variety of different products
  - LAN & μproc. shown here, but general application
  - Fixed problematic LAN & PLD products on old fab processes, as shown in Reliability Monitor Program
- Manuscript corresponding to this presentation can be found in the 2000 ESREF Proceedings, also as a Special Issue of Microelectronics Reliability, Vol 40, pp.1615-1618 (2000)