Magnetic Tunnel Junction RAM Reliability Issues

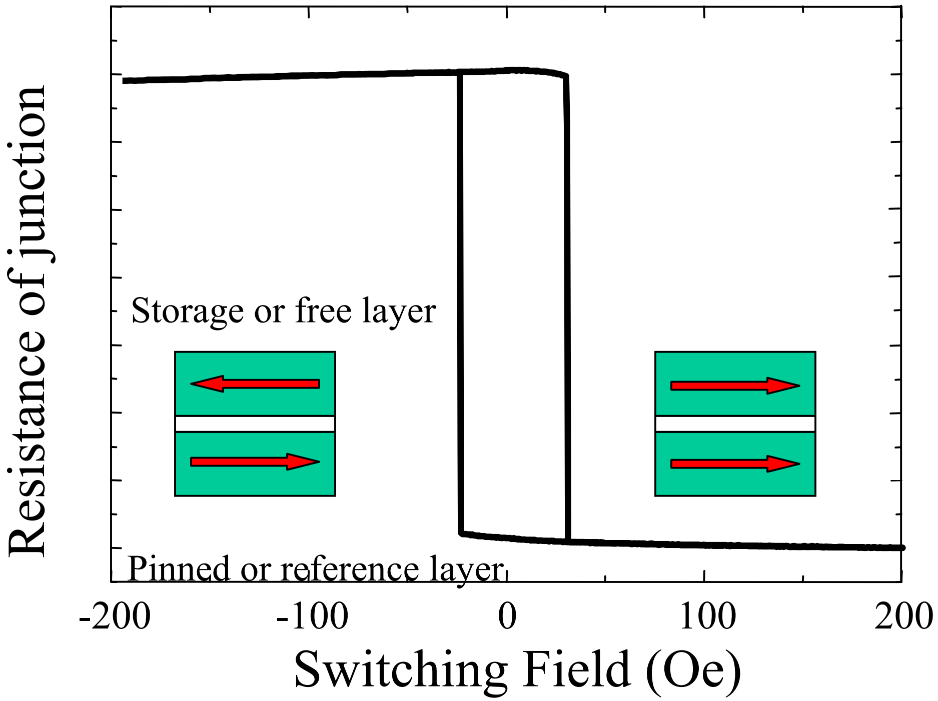
John Hummel and Carole Graas

MRAM Development Alliance, IBM/Infineon Technologies,
IBM Semiconductor Research and Development Center,
2070 State Route 52, Hopewell Junction, NY 12533, USA

Outline

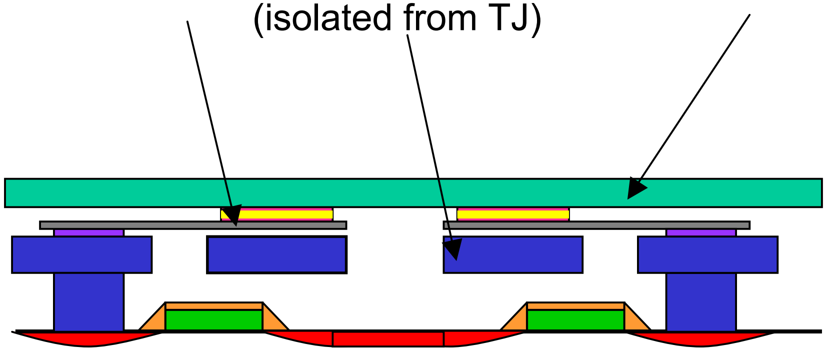
- MRAM Technology
  - Structure of MRAM device
    - magnetic tunnel junction structure
  - Operating parameters
    - current requirements
  - Reliability issues
    - structural issues- new materials and structures
    - sense issues - tunnel barrier reliability
    - write issues - interconnect reliability

MRAM Operation



- •Magnetic switching field is supplied by the current pulse in the WL and BL
- •Storage layer switches at low fields
- •Reference layer has higher coercivity and maintains reference orientation
- •Low resistance state has reference and storage layers with parallel magnetization
- •Magnetic stack contains several layers to tune and control magnetic properties

MRAM Device Structure



MTJ

Write
Word
Line
(isolated from TJ)

Bit
Line

Sense selection is by FET and
local interconnect to base of MTJ

- MRAM tunnel junction device is embedded in the BEOL interconnect structure
- device is switched by magnetic fields from current pulses in the WL and BL

Cross section of MTJ device

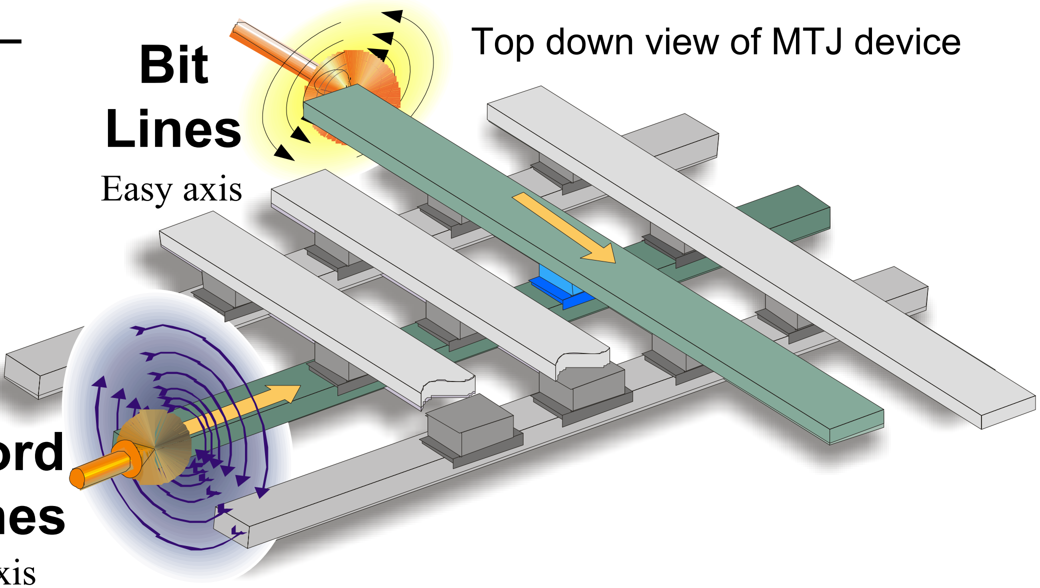
Storage layer

Reference
layer (SAF)

Hardmask

Tunnel barrier

Antiferromagnet



Top down view of MTJ device

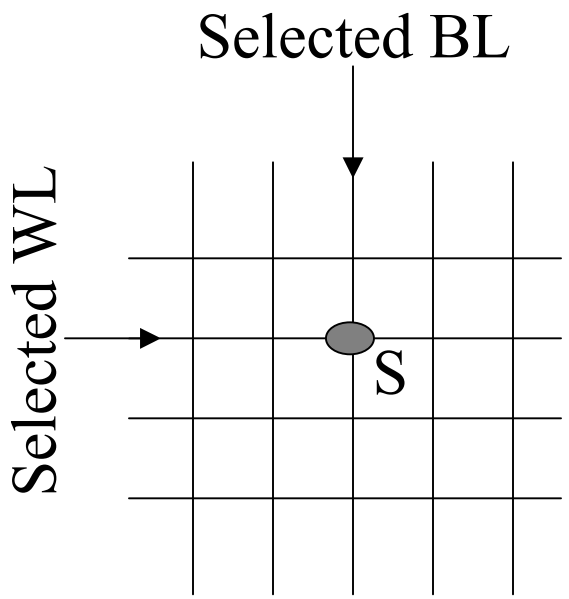
Bit Lines

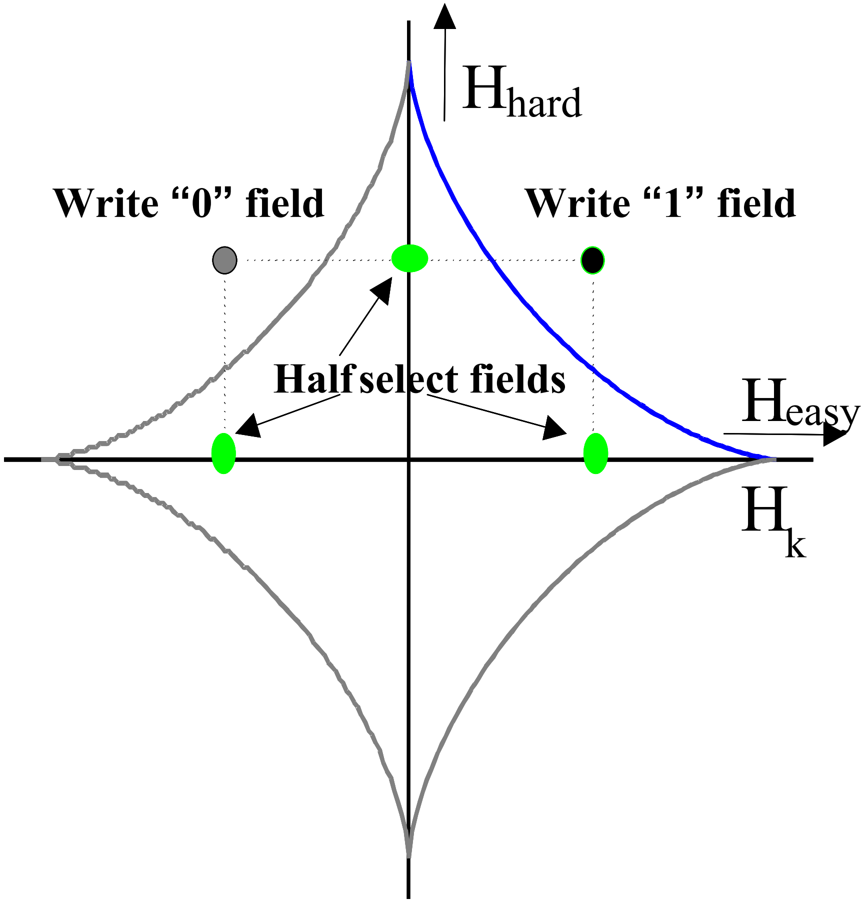
Easy axis

Word Lines

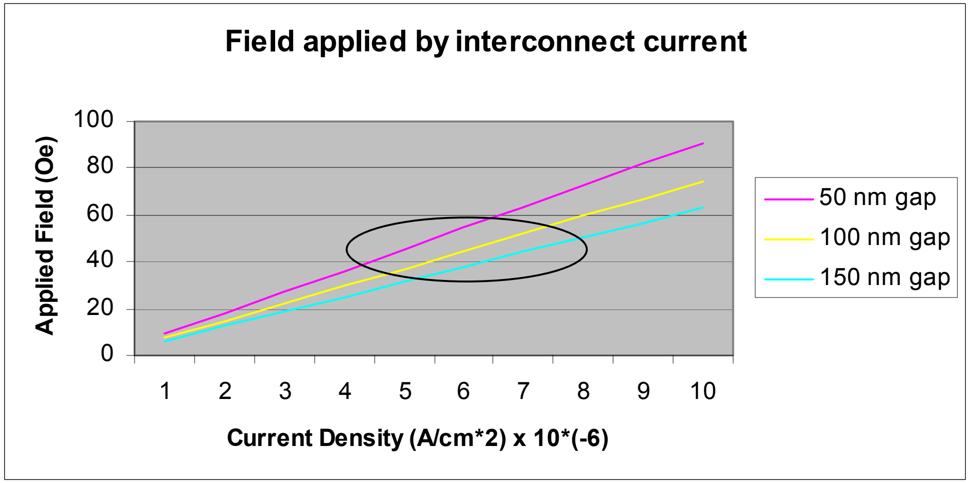
Hard axis

Coincident Field Selection for Writing MRAM



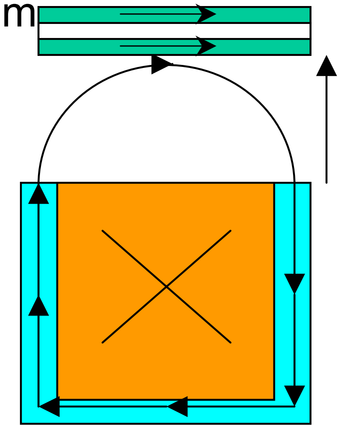


MRAM Device Switching - Writing



Current density (MA/cm^2) to provide required field

- Line width 0.25 um, AR 1.5
- distance from line to storage layer in range of 50-150 nm



Distance from write line to storage layer

Switching field and Activation Energy

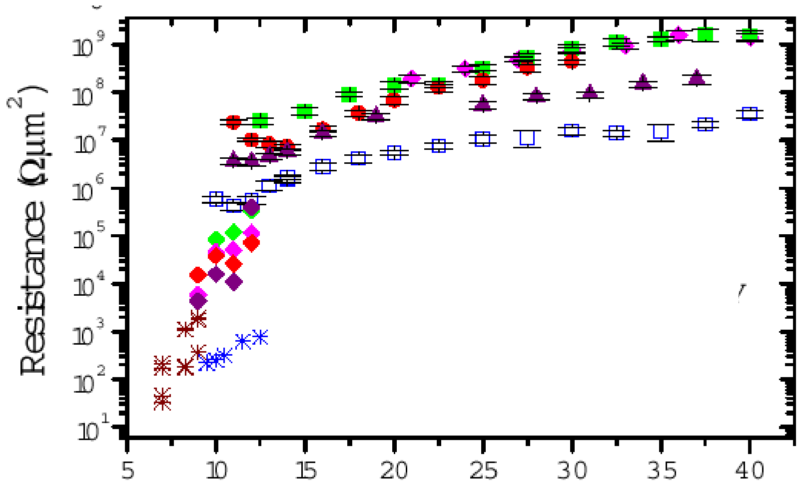
- $E_a(0) = (VM_sH_k/2)$
- $H_k \sim M_s(t/w(1-1/AR))$ AR - device aspect ration
  t= thickness, w= width
- For permalloy (t - 5nm, w - 400 nm, AR - 2)
  - $H_k \sim 60$ Oe
  - $Ea >> 100kT$

Use of ferromagnetic liner

"Keeper" cladding interconnect line can reduce current requirements:

current density can be reduced by a factor of at least 2X

Operating Conditions - Read

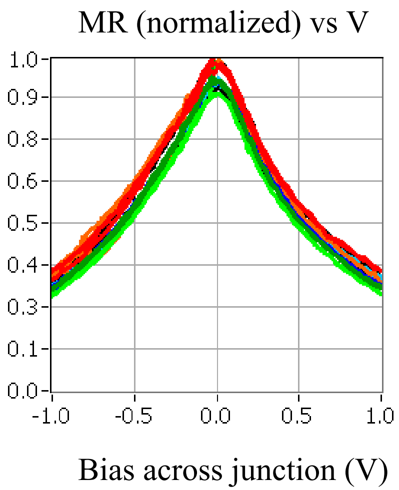


Al2O3 tunnel barrier thickness (A)
S.P.Parkin et al

Tunnel barrier resistance can be varied over wide range by increasing tunnel barrier thickness

Thickness control is a manufacturing issue since R increases by a factor of 2-3X per 0.1 nm

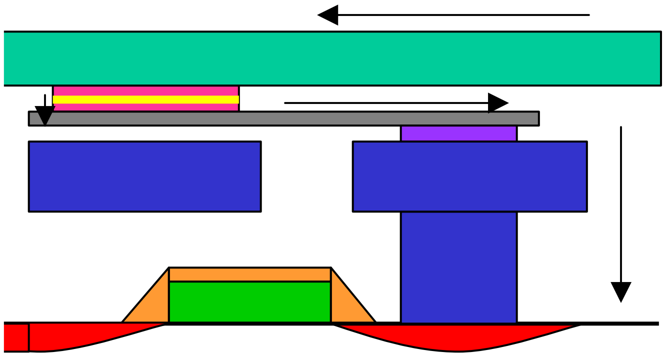
MRAM Device Structure (con't)



MR rolls off with increasing voltage, with approximately 50% drop at 0.5 V

MTJ resistance in the range of 10k-100kOhm for MRAM device

Sensing voltage presents tradeoff between sense signal and sense current



Sense operation through
BL, MTJ, local interconnect
to stacked via to FET

Key Reliability Concerns

Junction Issues (Sense):

- Sense operation involves resistance determination through the junction
  - MTJ area resistance product in range of 10*3 - 10*4 Ohm-um*2
- Bias across the 8-15A tunnel barrier determined by optimization of sense current and MR

Tunnel Barrier Reliability

- Evaluation of Al_2O_3 tunnel barrier reliability in ferromagnetic devices is in early stage
- Initial reports of degradation of stressed ferromagnetic tunnel junctions (De Boeck and Das et al. (2001 and 2002)) have been reported:
  - naturally oxidized Al_2O_3 from ~1 nm of Al
  - stressed at 1.35 V until breakdown
  - from Weibull plots

    β (2001) was reported to be 1.1, but with poor straight line fit possibly indicating extrinsic breakdown

    β (2002) was reported to be 0.3, with good fit to a straight line

    early fails (~1s) reported for both
  - Low β and early fails possibly due to junction fabrication processing or tunnel barrier deposition process

Key Reliability Concerns

Junction Issues (Programming):

- Half select conditions for threshold switching device:
    - asteroid defines switching threshold for programming - vector sum of hard and easy axis field below this value won’t switch device
    - half selected bits (along WL or BL) receive sub-critical field
    - variation in switching threshold (if shape control insufficient) can lead to inadvertent switching.

Key Reliability Concerns

Junction Issues (Programming):

- Interconnect reliability (EM)
  - current densities for writing can exceed J_{use} (DC defnition)
    - Joule heating becomes limiter for AC wiring
  - easy axis field applied by WL is intrinsically AC, since reference layer orientation field direction is determined by current pulse direction
  - hard axis field destabilizes the junction, could be DC
    - maintaining both WL and BL current as AC
    - maximum duty cycle for highest stress application - 30-50%

- Interconnect Reliability (SM/interface stability/ILD reliability)
  - lower temperature BEOL processing has been typically employed after the MTJ stack has been introduced into the BEOL structure
  - >300C processing has been demonstrated to reduce MR (Freitas)
  - most reports of MTJ stack have BEOL temperature (ILD deposition, etc) in the range of <350C
    - impact on industry standard copper processing and quality of ILD materials needs analysis
  - impact of lower temperature package/interconnect/anneals also requires study

Unique Materials and Structures

The MTJ stack obviously is composed of materials not typical in CMOS processing
ferromagnetic materials embedded in the interconnect structure may have adverse effects on interconnect and FEOL device reliability

Tunnel barrier
Al2O3, AlN, ZnS, …)

Storage layer (Co, Fe, Ni, …)

Reference layer or synthetic antiferromagnet (Co, Cu, Fe, Ni, Ru, …
Antiferromagnet (IrMn, PtMn, FeMn, PtMnCr…)

Encapsulation and adhesion/diffusion barriers are required to assure these materials do not interact with interconnect and are isolated from FEOL
- liners and barriers used for copper BEOL need to be evaluated

Summary

MRAM technology is maturing, discussions of key technology issues are increasing, and structures of initial implementation are becoming clearer

Tunnel junction resistance in the range of 10kOm-100kOhm required for MRAM application easily obtained with Al2O3 tunnel barrier

Centered, narrow distributions of switching field and narrow distributions of junction resistance are required and present challenges for manufacturability

Key reliability issues for the technology are:

- tunnel barrier lifetime, defect levels,
- impact of modified BEOL processes on FEOL device and BEOL structures
- isolation and encapsulation of magnetic materials with liner and ILD address same issues as containing Cu in Interconnects
- Switching fields need to be sufficient to avoid spontaneous switching yet provide controllable write margin at reasonable currents