Scaling and Technology Issues for Soft Error Rates

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This work was carried out by the Jet Propulsion Laboratory under contract with the National Aeronautics and Space Administration, Code AE as part of the NASA Electronic Parts and Packaging Program.
Outline

Space and Terrestrial Environments
  – Areas of overlap
  – Mechanisms and modeling

Experimental Results for DRAMs

Experimental Results for High-Speed Processors

SOI Technology

General Scaling Considerations

Conclusions
Environments for Atmospheric and Space Radiation

Atmospheric Radiation
  – High-energy neutrons from cosmic-ray interactions
    Secondary Process: recoil atoms from nuclear reactions
    Particles have short range
  – Alpha particles from radioactive impurities

Space Radiation
  – High-energy galactic cosmic rays
    Extremely energetic particles
    Produce ionization track with much higher track density than alpha particles
  – High-energy protons from trapped radiation belts

*High-energy neutrons and protons produce similar effects in silicon*
Energy Distributions of Atmospheric Neutrons and Protons in Earth-Orbiting Spacecraft

Space environments are less concerned with energies below 10 MeV due to shielding.
Direct and Indirect Processes

Each particle produces an ionization track

Most protons pass through the device with little effect

A few protons cause nuclear reactions

Short-range recoil produces ionization

a) Heavy ions (ionization by each particle)
b) Protons (nuclear reaction needed to produce recoil)
Radiation Tests for Space Applications

Particles with High dE/dx and Long Range
  – Yields effective area for interaction
  – Cross section increases to saturation value with high dE/dx

High-Energy Protons
  – Depends on sensitive volume
  – Affected by interactions in adjacent material
  – Recoil products have limited range
Charge Collection

Long-range particles produce more charge at short times as well as at long times.
Charge Collection Process

Bulk Substrate
- High charge density collapses field, producing “funnel”
- Diffusion allows charge collection well beyond depletion layer
- Diffusion length up to 50 µm in p-substrates

Epitaxial Substrate
- Charge effectively cut off by highly doped region beyond epi-layer
- Effective depth ~ twice epi-layer thickness for particles entering region at large angles
Charge collected in the capacitor and pass transistor both contribute to upset in DRAMs
Critical Charge Scaling for DRAMs

DRAM Upset Rates for Scaled Devices

Upset Rate from Heavy Ions Scales with Junction Area
  – Total cross section ~ chip area
  – Multiple-bit errors, device architecture are complications

Proton Upset Rate Is More Complex
  – Recoil atom range
    Short range for older processes
    Long range for newer processes
  – Distribution of recoil energies
The upset cross section at high LET exceeds the die area because of multiple-bit upset.
Proton upset in advanced DRAMs is markedly reduced compared to earlier technologies.
Energy Dependence of DRAM Upset

Energy dependence of proton upset does not change significantly for scaled devices at 256-Mb level.
Charge Collection in High-Performance Structures

Substrate and Isolation Well Affect Charge Collection
- High-performance devices usually have epitaxial substrates
- Design criteria differs from DRAMs
- Higher speed, less concern about power dissipation

Microprocessors Provide Benchmark for Comparison
- Dominated by registers and cache memory
- Transients in logic may become important for advanced devices
  Clocked logic is relatively immune to transients
### Threshold LET of Commercial Microprocessors

<table>
<thead>
<tr>
<th>Device</th>
<th>Manuf.</th>
<th>Year</th>
<th>Feature Size (approx.)</th>
<th>Threshold LET (MeV-cm²/mg)</th>
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<tbody>
<tr>
<td>Z-80</td>
<td>Zilog</td>
<td>1986</td>
<td>3 μm</td>
<td>1.5 - 2.5</td>
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<tr>
<td>8086</td>
<td>Intel</td>
<td>1986</td>
<td>1.5 μm</td>
<td>1.5 - 2.5</td>
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<tr>
<td>80386</td>
<td>Intel</td>
<td>1991</td>
<td>0.8 μm</td>
<td>2 - 3</td>
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<tr>
<td>68020</td>
<td>Mot.</td>
<td>1992</td>
<td>0.8 μm</td>
<td>1.5 - 2.5</td>
</tr>
<tr>
<td>LS64811</td>
<td>LSI</td>
<td>1993</td>
<td>1.2 μm</td>
<td>2 - 2.5</td>
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<tr>
<td>90C601</td>
<td>MHS</td>
<td>1993</td>
<td>1.2 μm</td>
<td>2 - 2.5</td>
</tr>
<tr>
<td>80386</td>
<td>Intel</td>
<td>1996</td>
<td>0.6 μm</td>
<td>2 - 3</td>
</tr>
<tr>
<td>PC603e</td>
<td>Mot.</td>
<td>1997</td>
<td>0.4 μm</td>
<td>1.7 - 3</td>
</tr>
<tr>
<td>Pentium</td>
<td>Intel</td>
<td>1997</td>
<td>0.35 μm</td>
<td>2 - 3</td>
</tr>
<tr>
<td>Power PC750</td>
<td>Mot.</td>
<td>2000</td>
<td>0.25 μm</td>
<td>2 - 2.5</td>
</tr>
</tbody>
</table>

*The threshold LET of microprocessors is essentially unchanged over many generations*
Energy Dependence of Proton Upset in Microprocessors

Proton Energy (MeV)

Cross Section (cm²/bit)

PC603e

Power PC 750
Effect of Scaling on Upset Rate

Critical Charge Decreases with Scaling
  – Higher speed
  – Lower switching voltage

Collected Charge also Decreases
  – Higher doping levels in channel region
  – Thinner charge collection depth (epitaxial layers)

Junction Area Is Lower
  – Area affects alpha, heavy ion responses
    Cross section depends on area
    Also affects charge collection
  – Proton upset depends on volume
Effect of Junction Area on Charge Collection from Alpha Particles

Silicon-on-Insulator Technology

Partially Depleted SOI Is Near-Term Technology
- Film thickness approximately 0.15 µm
- Reduces charge collection by ~ 10
- Fully depleted SOI has even smaller dimensions

No Radiation Data Available on Modern SOI Technology
- Substantial improvement in radiation susceptibility is expected
- Charge collection advantage partially offset by other factors
Radiation Test Results for Older SOI Technologies

Permanent Damage from Single Particles
A significant number of permanent errors are observed for advanced DRAMs.
Conclusions

Expected Device Scaling Trends are Inconsistent with Recent Proton Test Data

– 256-Mb DRAMs have significantly lower upset rates
– May be due to changes in capacitor storage technology
– Register upset rate in advanced microprocessors is also lower

Results Are Encouraging for Space Use as well as for Terrestrial Applications

– SOI technology will likely lead to even lower upset rate
– However, lower switching voltage and higher speed may reverse trend

Complex Device Architecture also a Factor in Advanced Devices

– Upset detection may not be straightforward
– Limits effectiveness of EDAC