Integration of Copper with Low-k Dielectrics for Advanced Interconnects

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Interconnect Performance Improvement

- Interconnect performance improvement requires the reduction of the resistance (R) and capacitance (C)
- Lower resistance (1997)
  - Al 0.25µm → Cu 0.22µm
- Lower capacitance (Today)
  - SiO₂ 0.22µm → FSG 0.18µm → SiLK™ dielectric 0.13µm

SiLK™ is a trademark of the Dow Chemical Co.
Elements Considered

- Customer requirements as a function of time
  - Performance, power, etc.
- Materials
  - Integration
  - Manufacturability
  - Extendibility
- Roadmap
## Dielectric Materials

<table>
<thead>
<tr>
<th>Materials</th>
<th>k</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon dioxide</td>
<td>3.9-4.5</td>
<td>PECVD</td>
</tr>
<tr>
<td>Fluorosilicate glass (FSG)</td>
<td>3.2-4.0</td>
<td>PECVD</td>
</tr>
<tr>
<td>Polyimides</td>
<td>3.1-3.4</td>
<td>spin-on</td>
</tr>
<tr>
<td>HSSQ</td>
<td>2.9-3.2</td>
<td>spin-on</td>
</tr>
<tr>
<td>Diamond-like carbon</td>
<td>2.7-3.4</td>
<td>PECVD</td>
</tr>
<tr>
<td>Carbon-doped SiO$_2$</td>
<td>2.7-3.3</td>
<td>PECVD</td>
</tr>
<tr>
<td>Parylene-N</td>
<td>2.7</td>
<td>CVD</td>
</tr>
<tr>
<td>Benzocyclobutenes</td>
<td>2.6-2.7</td>
<td>spin-on</td>
</tr>
<tr>
<td>Fluorinated polyimides</td>
<td>2.5-2.9</td>
<td>spin-on</td>
</tr>
<tr>
<td>MSSQ</td>
<td>2.6-2.8</td>
<td>spin-on</td>
</tr>
<tr>
<td>Aromatic thermosets</td>
<td>2.6-2.8</td>
<td>spin-on</td>
</tr>
<tr>
<td>Fluorinated DLC</td>
<td>2.4-2.8</td>
<td>PECVD</td>
</tr>
<tr>
<td>Parylene-F</td>
<td>2.4-2.5</td>
<td>CVD</td>
</tr>
<tr>
<td>Teflon AF</td>
<td>2.1</td>
<td>spin-on</td>
</tr>
</tbody>
</table>
Requirements For Low-k Materials

- Thermal stability to 400°C
- Dielectric constant below 3.0
- High glass transition temperature
- Low moisture absorption
- Good adhesion to caps, hardmasks, liners, etc.
- Good mechanical properties
- Chemical compatibility
- Solvent resistance
- High etch selectivity (RIE processing)
- Compatibility with CMP
- Commercially available with reasonable shelf-life
- Environmental compliance
- Low cost
### Dow Chemical SiLK™ Dielectric Properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant</td>
<td>2.62</td>
</tr>
<tr>
<td>Leakage current</td>
<td>$3.3 \times 10^{-10}$ A/cm² @ 1 MV/cm</td>
</tr>
<tr>
<td>Breakdown field</td>
<td>4 MV/cm</td>
</tr>
<tr>
<td>Tg</td>
<td>&gt; 450°C</td>
</tr>
<tr>
<td>Thermal stability</td>
<td>&gt; 425°C</td>
</tr>
<tr>
<td>Modulus</td>
<td>2.7 GPa</td>
</tr>
<tr>
<td>Toughness</td>
<td>0.62 MPam$^{1/2}$</td>
</tr>
<tr>
<td>Film Stress</td>
<td>45 MPa</td>
</tr>
<tr>
<td>Moisture uptake</td>
<td>0.25% @ 80% RH, 25°C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>0.18 W/mK</td>
</tr>
<tr>
<td>Crack growth rate in water (m/sec)</td>
<td>$&lt; 10^{-11}$ m/sec</td>
</tr>
</tbody>
</table>
Impact of SiLK™ Resin on Performance

- **Wire length** = 200µm
- **Driver resistance** = 500Ω
- **Wire width/space** = 0.225µm

- Al/Oxide: 11%
- Cu/Oxide: 17%
- Cu/FSG: 37%
- Cu/SiLK Resin:
CMOS9S BEOL Description

- Tungsten local interconnect level for increased wiring density
- Low-k ILD (SiLK™) used to reduce capacitance
  - First integration of Cu interconnects with low-k ILD
- 8 levels of Cu interconnects
  - Several BEOL options supported
    - 4 LVL-MT, 7LVL-2x FW, 8LVL-2x/4x FW
    - Dual damascene copper at all levels for reduced RPT
- Upper levels (FW) at 2x and 4x pitch
  - 2x pitch fatwires in USG/FSG bilayer (7LVL) and SiLK™ (8LVL)
  - 4x pitch fatwires in USG/FSG bilayer
- Minimum C4 pitch of 4 on 8
- Wirebond pitch of 60 µm in-line
Via Chain Cross Section
CMOS 9S0 Technology

<table>
<thead>
<tr>
<th></th>
<th>0.13 µm</th>
<th>0.18 µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDR shrink</td>
<td>0.25x</td>
<td>0.35x</td>
</tr>
<tr>
<td>supply voltage</td>
<td>1.2V</td>
<td>1.5V</td>
</tr>
<tr>
<td>gate length</td>
<td>0.125 µm</td>
<td>0.175 µm</td>
</tr>
<tr>
<td>(drawn)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1 pitch</td>
<td>0.35 µm</td>
<td>0.49 µm</td>
</tr>
<tr>
<td>M2 pitch</td>
<td>0.40 µm</td>
<td>0.63 µm</td>
</tr>
<tr>
<td>Mx pitch</td>
<td>0.45 µm</td>
<td>0.63 µm</td>
</tr>
<tr>
<td>2x pitch FW</td>
<td>0.90 µm</td>
<td>1.26 µm</td>
</tr>
<tr>
<td>4x pitch FW</td>
<td>1.80 µm</td>
<td>NA</td>
</tr>
<tr>
<td>metal levels</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>ILD</td>
<td>SilK™</td>
<td>USG/FSG</td>
</tr>
<tr>
<td>K_eff</td>
<td>3.0</td>
<td>4.0</td>
</tr>
</tbody>
</table>

9S BEOL Stack
8 Level Metal
(4@1x, 2@2x, 2@4x)
Electromigration Data

- e-flow from V1 to M2
- 295°C, 0.65E6 A/cm²

Graph showing cumulative failures (%) vs. time to failure (arb units) for SiLK ILD and Oxide ILD.
Reliability Elements Evaluated

BEOL Technology Reliability
* Electromigration
* Interlevel Dielectric, Time Dependent Dielectric Breakdown
* Intralevel Dielectric, Time Dependent Dielectric Breakdown
* Stress Migration
* Thermal Cycles
* T/H/B and BEOL Fuse
* Thermal Conductivity Measurements

C-4 Reliability
* Thermal Cycles
* T/H/B
* Chip pull
4-Level Metal SRAM Structure (3 in SiLK™)
6-Level Metal Structure (4 in SiLK™)

SiO₂

SiLK™ Polymer

Al

Cu
CMOS9S C4 Cross-section

Chip
Metal Layers (M1-M3 in SiLK, MT in Oxide)

Pb/Sn C4 Ball

Laminate Substrate

10 kV ×500 60.0 μm
Issues Encountered

- Material
  - SiLK™ semiconductor dielectric evaluated against a stringent set of requirements

- Process development
  - New dielectric material required development of new unit processes (i.e. dual hardmask patterning)

- New structures and ground rules were developed in order to deal with low modulus material
SiLK, HM2, HM1, ARC apply; Trough Lithography

Via Lithography

Via Etch

open ARC and HM2

open HM2

complete etch

clean, metallize, planarize, cap

pattern and etch troughs in HM1

Bilayer Hardmask Integration
Bilayer Hardmask Integration

pattern and etch troughs in HM1
via lithography

via etch

open HM2
complete etch

E. Barth
IBM Microelectronics
SRC-TRC on Reliability, 11/00
**Wirebond Damage**
CMOS9S "Sea-of-Vias" (SOV) Structure
Extendibility

- 0.13µm learning enables evolution to the 0.10µm generation
  - Unit processes, structures, etc. extendible to 0.10µm
- 0.10µm generation will require dielectric with k < 2.2
  - Porous dielectrics required to obtain ultra low-k
- Path to ultra low-k is spin apply
  - No known path to CVD ultra low-k
Summary

- IBM Microelectronics has introduced a 0.13µm BEOL technology with SiLK™ as the first true low-k ($k_{\text{eff}} = 3.0$) interlevel dielectric fully integrated with Copper wiring.

- This 0.13µm technology offers potential for high performance or low power products and will enable extendibility to the 0.10µm generation.

- IBM is already producing chips on an SRDC pilot production line, and plans to ramp up the technology on its high-volume Burlington, VT manufacturing lines in the first half of 2001.