On-Chip Thermal Engineering

Prof. Ken Goodson
Mechanical Engineering Department
Stanford University
# Micro Heat Transfer Lab

Ken Goodson, Stanford Mechanical Engineering

## Current Group

<table>
<thead>
<tr>
<th>Name</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sanjiv Sinha</td>
<td>Roger Flynn</td>
</tr>
<tr>
<td>Xuejiao Hu</td>
<td>Julie Steinbrenner</td>
</tr>
<tr>
<td>Sungjune Im (Materials Science)</td>
<td>Evelyn Wang</td>
</tr>
<tr>
<td>Kevin Ness</td>
<td>Ankur Jain</td>
</tr>
<tr>
<td>Jae-Mo Koo</td>
<td>Sebastien Vigneron</td>
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<tr>
<td>Yue Liang</td>
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<tr>
<td>Angela McConnell</td>
<td>Dr. Carlos Hidrovo</td>
</tr>
<tr>
<td>Eric Pop (Electrical Engineering)</td>
<td>Dr. Theresa Kramer</td>
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<tr>
<td>David Fogg</td>
<td>Dr. Ching-Hsiang Cheng</td>
</tr>
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## Recent Alumni

<table>
<thead>
<tr>
<th>Name</th>
<th>Institution</th>
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<tbody>
<tr>
<td>Prof. Mehdi Asheghi</td>
<td>Carnegie Mellon University (ME)</td>
</tr>
<tr>
<td>Prof. Dan Fletcher</td>
<td>UC Berkeley (Bioengineering)</td>
</tr>
<tr>
<td>Prof. Bill King</td>
<td>Georgia Tech (ME)</td>
</tr>
<tr>
<td>Prof. Katsuo Kurabayashi</td>
<td>University of Michigan (ME)</td>
</tr>
<tr>
<td>Prof. Sungtaek Ju</td>
<td>UCLA (ME)</td>
</tr>
<tr>
<td>Prof. Kaustav Banerjee</td>
<td>UC Santa Barbara (EE)</td>
</tr>
<tr>
<td>Dr. Uma Srinivasan</td>
<td>Xerox</td>
</tr>
<tr>
<td>Dr. Per Sverdrup</td>
<td>Intel</td>
</tr>
<tr>
<td>Dr. Peng Zhou</td>
<td>Cooligy</td>
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<tr>
<td>Dr. Maxat Touzelbaev</td>
<td>AMD</td>
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</tbody>
</table>

On-Chip Thermal Resistances

\[
C_{\text{interconnect}} \quad T_{\text{interconnect}} \quad q_{\text{interconnects}} \quad R_{\text{interconnect}}
\]

\[
C_{\text{transistor}}
\quad T_{\text{transistors}}
\]

\[
C_{\text{chip}}
\quad T_{\text{chip}}
\]

\[
C_{\text{heat sink}}
\quad T_{\text{spreader}}
\]

\[
R_{\text{chip} + \text{TIM}}
\]

\[
R_{\text{heat sink}}
\]

\[
T_{\text{ambient}}
\]

Device-Level SEM

- metal
- ILD
- IBM

chip carrier

Si chip

heat spreader

heat sink

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On-Chip Thermal Challenges

$$\text{Peak } \Delta T \sim \bar{j}^2 \frac{d_m \rho_m d_d}{k_d} N^2$$

~30°C at 70 nm node
~80°C at 50 nm node

Global Wires

Interconnect Temperature Field

Student: Sungjun Im, Proc. IEDM 2000

Silicon

interconnect self heating

$$R_{\text{interconnect}}$$


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On-Chip Thermal Challenges

microprocessor hotspots (mm scale)

interconnect self heating

R_{chip + TIM}

R_{interconnect}


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On-Chip Thermal Challenges

transistor hotspots (nm scale) $R_{\text{transistor}}$

microprocessor hotspots (mm scale) $R_{\text{chip} + \text{TIM}}$

interconnect self heating $R_{\text{interconnect}}$

ITRS transistor in 2010

On-Chip Thermal Challenges

IBM

November 11, 2002
IBM's 3D IC: No Funny Glasses Needed
By Clint Boulton
Laying claim to an important step along the path to creating mightier integrated circuits (ICs), IBM (Quote, Chart) Monday said it has crafted a new technique for building three-dimensional ICs that will help increase chip performance, functionality and density.

Researchers at IBM's Research Division lab in Yorktown Heights, N.Y. explained that current

DARPA 3D-IC Program, 2004-2008

100+ Layers of logic & memory!


TRC: Oct 25-27, 2004

Stanford University
Outline

• Transistor hotspots
• Interconnect self heating
• Nano-engineered interface materials
• Electroosmotic microfluidic cooling
On-Chip Thermal Challenges

Bulk FET

SOI/SiGe

FinFET

Carbon nanotube transistor


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Transistor Thermal Processes

High Electric Field

Hot Electrons (Energy E)

\( E > 50 \text{ meV} \quad \tau \sim 0.1\text{ps} \)

\( E < 50 \text{ meV} \quad \tau \sim 0.1\text{ps} \)

Optical Phonons

\( \nu_{op} \sim 1000 \text{ m/s} \)

Acoustic Phonons

\( \nu_{ac} \sim 9000 \text{ m/s} \)

Heat Conduction to Package

\( \tau \sim 10 \text{ ps} \)

\( \tau \sim 1 \text{ ms} - 1 \text{ s} \)

IBM

Source

Gate

Drain

Stanford University

IBM

Heat Conduction to Package

Optical

Acoustic

TrC: Oct 25-27, 2004

SemaTech
Transistor Simulation Regime Map

Phonons
- Atomistic
- BTE with Atomistic Models
- BTE or Monte Carlo
- Diffusion

Available Software

Transistor Requirements
<table>
<thead>
<tr>
<th>electrons</th>
<th>phonons</th>
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</thead>
<tbody>
<tr>
<td>MFP</td>
<td>~5 nm</td>
</tr>
<tr>
<td>λ</td>
<td>~5 nm</td>
</tr>
</tbody>
</table>

Currently Available

Electrons

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Transistor Simulation Regime Map

Phonons
- Atomistic
- BTE with Atomistic models
- BTE or Monte Carlo
- Diffusion

Currently Available
- atomistic hotspot relaxation calculations
- split flux phonon BTE

Electrons
- Drift Diffusion
- BTE Moments
- Monte Carlo & BTE
- Monte Carlo with Quantum Models
- Full Quantum

Stanford Research
- Electron Monte Carlo with phonon dispersion & branch accuracy

MONET

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TRC: Oct 25-27, 2004
2D Monte Carlo of 18 nm Thin-Body SOI Transistor

**ITRS Specs:**
- \( L_G = 18 \text{ nm}, \ t_{SI} = 4.5 \text{ nm}, \ t_{OX} = 1 \text{ nm} \)
- \( N_{SD} = 1 \times 10^{20} \text{ cm}^{-3}, \ N_{CH} = 1 \times 10^{15} \text{ cm}^{-3} \)
- \( I_{ON} = 1000 \ \mu A/\mu m, \ I_{OFF} = 1 \ \mu A/\mu m \)
- \( \Phi_{GATE} = 4.53 \text{ eV (Mo)}, \ V_{DD} = 0.8 \text{ V} \)

*if \( W/L = 4 \) then \( N_{elec} \sim 2500 \text{ total!} \)*

Thesis work of Eric Pop, 2004  Stanford University
Phonon Spectrum in 1D Hotspot

Sinha & Goodson, Proc. THERMINIC 2004, also see review to appear in the International Journal of Multiscale Computational Engineering
Hotspot Temperature

Based on ITRS 2003

1 Based on ITRS 2003

Year¹

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Outline

• Transistor hotspots
• Interconnect self heating
• Nano-engineered interface materials
• Electroosmotic microfluidic cooling
Interconnect Self Heating

Student: Sungjun Im. Sponsor – MARCO IFC

Compounding ITRS trends lead to accelerating peak temperature:
- low-k dielectric materials with poor thermal conductivities
- increasing current densities and aspect ratios
- increasing number of interconnect layers

\[ \text{Peak } \Delta T \sim \bar{j}^2 \frac{d_{\text{MET}} \rho_{\text{MET}}}{k_{\text{ILD}}} \frac{d_{\text{ILD}}}{\eta} N^{1.7} \]

Temperature Contour Plot
(50 nm technology node)

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Via Hotspots

S. Im, K. Banerjee, and K. E. Goodson, IRPS 2002. Sponsor: MARCO IFC

Via and interconnect dimensions are not consistent from a heat generation / thermal resistance perspective, leading to hotspots. New model accounts for via conduction and Joule heating and recommends dimensions considering temperature and EM lifetime.

Based on ITRS global lines of a 100 nm technology node
(Left: ANSYS simulation. Right: Closed-Form Modeling)
Outline

• Transistor hotspots

• Interconnect self heating

• Nano-engineered interface materials

• Electroosmotic microfluidic cooling
Carbon Nanotubes in Thermal Interface Materials

Students: Xuejiao Hu, Angela McConnell, Antonio Padilla, Senthil Govindasamy
Sponsors: SRC, Intel, IBM, Raytheon, Molecular Nanosystems

- **Homogeneous mixture with particles**
  Hu, Jiang, and Goodson, Itherm 2004, SRC patent pending

- **Aligned growth (one side)**
  Hu, Padilla, Xu, Fisher and Goodson
  Submitted to Semitherm 2005

- **Aligned growth (two sides, “thermal nano velcro”)**
  Work in progress! In collaboration with Dai’s group, Stanford
Homogeneous CNT-Particle Mixture

Hu, Padilla, Goodson, Proc. THERM 2004

SEM image of a composite with nickel spheres and CNTs in a silicone matrix

Experimental Results

Traditional TIMs

CNTs

Nickel

Silicone

$\frac{k_{TIM}}{k_{silicone}}$

CNT Volume Fraction

40% Ni

30% Ni

0% Ni

0.00 0.01 0.02 0.03

Experimental Results
Aligned CNTs on Silicon

Hu, Padilla, Xu, Fisher, Goodson, submitted to SEMI-THERM 2005
Stand-alone Single-walled CNT

McConnell, Jiang, and Goodson, NSF Design, Service & Manufacturing Grantees and Research Conference, 2004
Outline

• Transistor hotspots
• Interconnect self heating
• Nano-engineered interface materials
• Electroosmotic microfluidic cooling
Thermal Management Challenge

Microprocessor heat sinks are 3000 times larger and heavier than the chip. They crowd away power delivery components, ASICs, RAM, and Video.

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“Dream Heat Sink” (1998 Brainstorm)

- no larger or heavier than microprocessor chip
- targeted cooling at hotspots
- fully-integrated, silent, reliable pump
- temperature sensors control pump flowrate
Modular EO Microchannel Cooling System


Heat Rejector
- ElectroOsmotic Pump
- High-Pressure Liquid Pumping
- Silicon dioxide wall
- Charge double-layer

Micro Heat Sink
- EO Pump
- 3D Microchannel Heat Sink

PIs: Goodson, Santiago, Kenny, Stanford

Sponsors: DARPA, Intel, AMD, Apple

TRC: Oct 25-27, 2004

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ElectroOsmotic Pumps

With groups of Santiago and Kenny, Stanford Mechanical Engineering
Sponsor: SRC/MARCO, DARPA, Intel

Idealized pore channel:
Glass or fused-silica capillary wall

\[ u(r) = \frac{\varepsilon \zeta E}{\mu} - \frac{dp}{dx} \left(a^2 - r^2\right) \]

\[ Q_{\text{max}} = \frac{\varepsilon \zeta}{\mu} \frac{VA}{l} \quad \Delta p_{\text{max}} = \frac{32\varepsilon \zeta}{d^2} V \]

- Very high volume to flowrate ratio
- Stanford pump performance (Feb 2003):
  \( P_{\text{max}} \sim 2 \text{ atm}, \quad Q_{\text{max}} \sim 40 \text{ ml/min}, \quad \text{Vol.} \sim 2 \text{ cm}^3 \)

Silicon micromachined pump

Free-standing pump

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EO Microchannel Cooling

Stanford/DARPA/Intel Demo, 2002

<table>
<thead>
<tr>
<th>Total Power</th>
<th>Peak Heat Flux</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>200</td>
<td>50</td>
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</table>

- DARPA Launch
- High-Flow Frit pumps
- Micro hx CAD
- Integrated Demos

1999 2000 2001 2002 2003 2004 2005

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EO Microchannel Cooling

Zhou, Upadhya, Goodson, Munch, *Proc. Semitherm 2004*

See also Upadhya et al., *ITHERM 2004*

<table>
<thead>
<tr>
<th>Year</th>
<th>DARPA Launch</th>
<th>Heat rejector</th>
<th>Micro hx</th>
<th>CAD</th>
<th>Integrated Demos</th>
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<tr>
<td>1999</td>
<td>10</td>
<td>30</td>
<td>100</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td>10</td>
<td>30</td>
<td>100</td>
<td>50</td>
<td></td>
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</table>

Total Power

Peak Heat Flux

10     30     100     200
10     30     100     50

Cooligy, Inc.

150 W
500 W/cm²

Integrated Prototype Product Shipment

1999 2000 2001 2002 2003 2004 2005

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TRC: Oct 25-27, 2004
Microchannel Research Trajectory

mixed signal I/O module releases chip backside for RF, Photonic, MEMS I/O using Integrated electrical/fluidic interconnects

Research Background

DARPA Heretic
Intel
AMD
Apple

Through-Wafer Electrical I/O

Mixed Signal Chip

Photonic I/O
RF
Integrated MEMS Sensing
Fluidic I/O

Cooling

1999 2000 2001 2002 2003 2004 2005

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TRC: Oct 25-27, 2004
Microchannel Research Trajectory

Vertical Fluidic Microchannels at Chip Corners

Interconnect Layers

Device Layers

Fluidic Microchannel Cooling Layers

Vertical Metallic Via

Lateral Metallic Heat Spreading Structure

Fluidic Microchannel

3D IC Cooling

DARPA 3DIC

1999 2000 2001 2002 2003 2004 2005

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Integrated Electrical & Thermofluidic Interconnects


Lateral Channel Formation
Oxide deposition
Pattern and etch
Epi-silicon encapsulation
CMP planarization

Vertical Through-wafer Interconnects
DRIE
Thermal oxidation
Nitride deposition
Polysilicon deposition and doping
Polysilicon via fill
CMP
Polysilicon deposition and doping and pattern

Fluidic Channel Release
Oxide etch to fluidic channels
HF vapor etch of oxide filled channels
LTO sealing
Fluidic connection

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Concluding Remarks

• On-chip thermal engineering is coming of age, with critical challenges posed by interconnect self heating and nanoscale transistor hotspots. These challenges are aggravated by exploratory materials and geometries including SiGe, SOI, FinFETs, and low-k dielectrics.

• Pumped fluidic cooling systems will soon be the commercial standard for workstations and desktops, and this motivates the design of optimal microfluidic heat sinks and pumps. Trends to circuit hyperintegration including 3D geometries are hastening the need for chip-integrated microfluidics.