The Trend of TSV Packaging

Dr. ChoonHeung Lee
Amkor
Package Trend

Small form factor or cost

I/O numbers or performance >> >>
Packages Growth Rate

<table>
<thead>
<tr>
<th>Surface Mount PKG (SO, PLCC, QFP, QFN)</th>
<th>Modules (TAB, COF, COB, DCA)</th>
<th>FC BGA / PGA / LGA</th>
<th>FC CSP</th>
<th>WB BGA / CSP</th>
<th>Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>13.8%</td>
<td>7.1%</td>
<td>3.8%</td>
<td>25.8%</td>
<td>7.8%</td>
<td>13.3%</td>
</tr>
</tbody>
</table>

2010 OSAT Revenue: $23.6B

2015 OSAT Revenue: $32.7B

* Source: Gartner Dataquest (Oct.'11), Prismark (Aug.'11), Amkor Estimates
3D Packaging Paradigm Change

- **Package Stacking**
  - Package-on-Package
  - Package-in-Package

- **3D Stacking**
  - Flip chip + Wire bonding
  - Wire bonding + Wire bonding

- **3D IC**
  - TSV
3D-TSV IC Technology Tree

- Memory Stack
  - Performance
  - Form Factor

- Wide IO
  - Performance
  - Low Power
  - Form Factor

- Logic + Memory
  - Performance
  - Form Factor

- FPGA
  - Performance

Drive Force

- Vertical Via Technology
- Wafer Technology
- Stacking Technology

Direct Vertical Stack

Interposer use side by side
Several News in TSV Area

TSMC reveals plan for 3DIC design based on silicon interposer & TSV(Jun 8th 2010)

Elpida, PTI & UMC to partner for 3DIC commercialization of logic+DRAM stack with 28nm by 2011(Jun 23rd 2010)

3DIC memory with wide I/O interface is coming by 2013, says NOKIA (Sep 17th 2010)

Xilinx brings 3D TSV interconnects to commercialization phase in digital FPGA world (Oct 27th 2010)

Micron reveals “Hyper Memory Cube” 3DIC technology (Feb 18th 2011)

Samsung wide I/O memory for mobile products – A deeper look (Feb 28th 2010)
TSV Packaging Process

- TSV Wafer Prepare
- Carrier Wafer Attach
- Wafer Grinding
- Wafer RDL / Bumping
- Carrier Wafer Detach
- Chip on Substrate
- Chip Stacking – 3D
- 3D Finalizing
2.5D Interposer TSV
3D IC Technology

Vias “First”

Front-End FAB Process

Vias drilled in bare Si
Vias filled with Poly-Si
Possible via resistance issues

Vias “Early/Middle”

Front-End FAB Process

W-CVD or Cu plated

Vias “Last” – Back Side

OSAT Process

Active Interposer

Passive Interposer

Passive Interposer substrate
Interposer Technology

Front-side BEOL

Active or Passive Component (optional)

Substrate (Glass or Silicon)

TSV

Back-side RDL

Bumps or Copper pillars (100-200μm pitch)

UBM (under Bump Metallurgy)

Metal (Al or AlSiCu, or Cu or W)

ILD (Inter Layer Dielectric, SiO2 or Si3N4 or polymer...)

Dielectric passivation (Polyimide, BCB, epoxy, AL-X)

Source: Yole

© Fraunhofer IZM
Interposer Supply Chain – Logistics

**Business Concerns:**
- Ownership of TSV related failures
- Cost
- Agreed to metric for good known good Wfr

**Technical Concerns:**
- BOM Compatibility
  - Same bump metallurgies
  - Same passivation materials
- Thin wafer handling / shipping

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**Wafer Finish – Can be at either Foundry or OSAT**

1. **Foundry/IDM** → **Vias Early** → **Front Side NiPdAu Pad**
2. Continue at Foundry
   - **Wfr Support** → **Thin** → **Back Side Bump** → **Debond** → **Ship**
3. **Send to SAT**
   - **Wfr Support** → **Thin** → **Back Side Bump** → **Debond**
4. **Assy**
Who Is Doing What?

TSV
- Corning
- HOYA
- Nippon Electric Glass

RDL
- Unimicron
- IBI
- IBIDEN
- DNP
- SHINKO

Bumping
- TSMC
- GLOBAL FOUNDRIES
- DALSIA
- Silex Monosystems
- ipdia
- UMC
- ALLVIA

Packaging
- Amkor Technology
- SPIL
- STATSchipPAC
- Powertech
- ASE Group

Test
- Samsung
- Texas Instruments
- ST
- NXP
- IBM
- Toshiba
- Infineon
- Sony

Source: Yole, 2010
Interposers Increase Logic Capacity while Reducing Power

- Higher yields
- Over 2X FPGA capacity advantage
- 50% power reduction from 40nm FPGAs
- 5X reduction in latency
- 100X improvement in inter-die bandwidth/watt
- Passive silicon interposer
  : Minimizes heat flux issues
  : 20X denser wire pitch
  : 65 nm technology

The Cost of TSV Is Compatible with the Application Markets?

Example: XILINX VIRTEX 5 market price

![Xilinx Virtex 5 Market Price Table]

- XC5VLX220-2FF1760I: $6749.75
- XC5VLX220-2FFG1760I: $6482.25
- XC5VLX220-2FFG1760I: $5649.75
- XC5VLX220-1FF1738I: $4475.45
- XC5VLX220-1FFG1738I: $3816.33

Example: nVidia market price

- nVidia Quadro 2000 is priced at $600
- nVidia Quadro 4000 is priced at $1000
- nVidia Quadro 5000 is priced at $2500
Si Interposer Substrate: ‘A Si Interposer BGA PKG with Cu-filled TSV and Multi layer Cu Plating Interconnect’, Kouichi Kumagai et al, 2008 ECTC

Table 1  TEST Chip Specifications

<table>
<thead>
<tr>
<th>SiP PKG</th>
<th>144pin BGA (12x12 Ball Array)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiP</td>
<td>Body size: 11 mm x 11 mm</td>
</tr>
<tr>
<td>TSV</td>
<td>Thickness: 200µm</td>
</tr>
<tr>
<td>TSV</td>
<td>Pitch (Outer ball pitch): 800µm</td>
</tr>
<tr>
<td>Cu RDL</td>
<td>Diameter: 60µm</td>
</tr>
<tr>
<td>Cu RDL</td>
<td>Layer: 2</td>
</tr>
<tr>
<td>Cu RDL</td>
<td>Line / Space (Min.): 4µm / 4µm</td>
</tr>
<tr>
<td>Cu RDL</td>
<td>Cu Thickness: 3µm</td>
</tr>
<tr>
<td>Cu RDL</td>
<td>Via Diameter: 10µm</td>
</tr>
<tr>
<td>FC Mounted Chips</td>
<td>4-chip Common</td>
</tr>
<tr>
<td>Chip size</td>
<td>3.35 mm x 3.1 mm</td>
</tr>
<tr>
<td>Technology</td>
<td>0.5µm CMOS, 3ML</td>
</tr>
<tr>
<td>Thickness</td>
<td>200µm</td>
</tr>
<tr>
<td>Micro-bump pitch</td>
<td>50µm (Chip 1,3,4), 40µm (Chip 2)</td>
</tr>
<tr>
<td># of micro-bumps</td>
<td>Chip 1: 2,964</td>
</tr>
<tr>
<td># of micro-bumps</td>
<td>Chip 2: 4,615</td>
</tr>
<tr>
<td># of micro-bumps</td>
<td>Chip 3: 2,029</td>
</tr>
<tr>
<td># of micro-bumps</td>
<td>Chip 4: 1,886</td>
</tr>
</tbody>
</table>

Fig. 3  TEST Chip Top View
Si TSV Interposer RF Module

RF Mobile Transceiver (2.4 x 3.6 mm²)
SnAg Solder Bumps (diameter: 50 µm)
Si Carrier (300 µm thickness)
TSV (8x8x 300 µm)
RDL Cu 20 µm line /space
Solder Balls (diam. 250 µm /500 µm pitch)
3D Interposer Wafer Forecast by Application

Source: Yole, 2010

<table>
<thead>
<tr>
<th>Year</th>
<th>Memory only interposers</th>
<th>RF / Power / Analog passive interposers</th>
<th>HB-LED interposers</th>
<th>CMOS image sensor interposers</th>
<th>Logic+memory interposers</th>
<th>Logic-only interposers</th>
<th>MEMS &amp; Sensors interposers</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>32</td>
</tr>
<tr>
<td>2010</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>46</td>
</tr>
<tr>
<td>2011</td>
<td>1</td>
<td>7</td>
<td>1</td>
<td>8</td>
<td>0</td>
<td>0</td>
<td>74</td>
</tr>
<tr>
<td>2012</td>
<td>4</td>
<td>14</td>
<td>5</td>
<td>34</td>
<td>0</td>
<td>0</td>
<td>124</td>
</tr>
<tr>
<td>2013</td>
<td>7</td>
<td>26</td>
<td>13</td>
<td>97</td>
<td>18</td>
<td>9</td>
<td>182</td>
</tr>
<tr>
<td>2014</td>
<td>13</td>
<td>47</td>
<td>28</td>
<td>207</td>
<td>52</td>
<td>63</td>
<td>282</td>
</tr>
<tr>
<td>2015</td>
<td>29</td>
<td>80</td>
<td>62</td>
<td>371</td>
<td>243</td>
<td>685</td>
<td>389</td>
</tr>
</tbody>
</table>
3D Device TSV
Mobile Applications

Wide I/O memory die (~1200ubumps, no TSV)
28node (Cu pillar, 10um dia. TSV)
Substrate (14 x 14 /12 x 12 mm)
Die 2 Substrate interconnection : TCNCP
Die 2 Die interconnection : TCNCP
Heat spreader attach (exposed die molding) :optional
Band Width Limit vs. Cost Budget

Affordable Cost
For the performance

$50(?)

$30

$20
The Cost of TSV Is Compatible with the Application Markets?

iPad2 BOM/Cost Analysis by iSupply April 2010

<table>
<thead>
<tr>
<th>Component Description</th>
<th>Supplier/Manufacturer</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery - Li-ion Polymer, 3.75V, 6600mAh</td>
<td>Amperex Technology, Dynapack</td>
<td>$21.00</td>
</tr>
<tr>
<td>Microprocessor A4 Microprocessor Core Integrated with Graphics Processing Unit w/ PoP DRAM</td>
<td>Designed by PA Semiconductor, Manufactured by Samsung</td>
<td>$19.50</td>
</tr>
<tr>
<td>2Gbit Mobile SDRAM - Package on Package (stacked on A4)</td>
<td>Samsung</td>
<td>$7.30</td>
</tr>
<tr>
<td>WLAN n + BT + FM Module (Featuring Broadcom)</td>
<td>Broadcom</td>
<td>$8.05</td>
</tr>
</tbody>
</table>

Quad core AP + wide I/O memory price is assumed as $50

Dual core AP + LPDDR2 price is $20~$30
Memory Applications

- **DDR3 4Gb DIMM (1.066GHz) for server application is around $250**
- **DDR3 4Gb for PC is around $20**
### 3D TSV Applications

Key to 3D commercialization is a cost/performance ratio!

<table>
<thead>
<tr>
<th>Application</th>
<th>Driver</th>
<th>Status</th>
<th>Barrier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Image sensors</td>
<td>Performance, Form factor</td>
<td>Production</td>
<td>None</td>
</tr>
<tr>
<td>CPUs + memory</td>
<td>Performance</td>
<td>16nm Si node or beyond</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>GPUs + memory</td>
<td>Performance</td>
<td>2014</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>FPGAs</td>
<td>Performance</td>
<td>2014</td>
<td>Cost, process, yield, infrastructure</td>
</tr>
<tr>
<td>Wide I/O memory with processor</td>
<td>Performance (bandwidth extension, lower power consumption), Form factor</td>
<td>2012~13</td>
<td>Cost, process, yield, KGD, infrastructure (including business logistics)</td>
</tr>
<tr>
<td>Memory (stacked)</td>
<td>Performance, Form factor (z-height)</td>
<td>2012</td>
<td>Cost, process, yield, assembly</td>
</tr>
</tbody>
</table>

Source: TechSearch, 2011
Thank you