Technical Challenges in TSV Integration to Si

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Electronics Industry Trends

High Density / High Speed / Low Power
Scaling continues, but is getting more and more difficult & expensive !!!
3-D TSV Technology

- 3-D TSV is an alternative solution!!!

- Small form-factor
- Higher performance
- Lower power consumption
- Multi-function integration
- Cost effective (?)
TSV Applications: Stacked Memories

- In 2006, the development of wafer-level processed stack package (WSP) of high-density memory chips using TSV interconnection technology.

- Aug 2011, 32GB DDR3 RDIMM using 3D TSV technology.
TSV Applications: CIS & Logic

**TSV for CMOS Image Sensors**
- Via Last
- Mass Production (2008~)

**TSV for Logic Applications**
- Via Middle
- Memory on Logic & Si-Interposer
Why TSVs?

- Mobile AP Bandwidth Requirement

Bandwidth requirement is doubled by every year

→ Wide I/O is the solution!!! → TSVs are needed
Great Combination: Wide I/O + TSV

- Best of both worlds
  - Wide I/O: For performance
  - TSV (Through Silicon Via) for Thinnest multiple-die stack

![Wide I/O + TSV Diagram]

![Size, Power & Speed Diagram]
Wide I/O DRAM

- Mobile Wide I/O DRAM capable of 12.8GB/s data transfer

*FEB, 2011*

12.8GB/s through x512 I/Os

<table>
<thead>
<tr>
<th></th>
<th>Conventional 3D Package (FC-PoP) with LPDDR2</th>
<th>TSV-SiP with Wide I/O memory</th>
</tr>
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<tbody>
<tr>
<td>Memory I/O Power Consumption</td>
<td>176 mW</td>
<td>44 mW</td>
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Introduction

Challenges in TSV Process

- TSV Process Flow & Key Technologies
- Issues in TSV Integration to Si
  - TSV Impact on BEOL
  - TSV Impact on FEOL
  - TSV Yield

Conclusions
## 3-D TSV Process Options

<table>
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<tr>
<th>Process</th>
<th>Options</th>
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<tr>
<td><strong>TSV drilling</strong></td>
<td>Bosch DRIE</td>
</tr>
<tr>
<td>Non-Bosch DRIE</td>
<td>Laser</td>
</tr>
<tr>
<td><strong>TSV side wall insulation</strong></td>
<td>SiO2</td>
</tr>
<tr>
<td>Polymer</td>
<td></td>
</tr>
<tr>
<td><strong>TSV-filling conductor</strong></td>
<td>poly-Si</td>
</tr>
<tr>
<td>Cu</td>
<td>W</td>
</tr>
<tr>
<td><strong>TSV process flow</strong></td>
<td>Vias First</td>
</tr>
<tr>
<td>Vias Middle</td>
<td>Vias Last backside</td>
</tr>
<tr>
<td>Vias Last frontside</td>
<td></td>
</tr>
<tr>
<td><strong>Stacking</strong></td>
<td>Wafer to wafer</td>
</tr>
<tr>
<td>Chip to wafer</td>
<td>Chip to substrate</td>
</tr>
<tr>
<td><strong>Bonding</strong></td>
<td>Direct oxide</td>
</tr>
<tr>
<td>Polymer</td>
<td>Cu-Cu thermo-compression</td>
</tr>
<tr>
<td>IMC</td>
<td>Hybrid Direct bond</td>
</tr>
<tr>
<td><strong>Thin wafer handling</strong></td>
<td>On carrier</td>
</tr>
<tr>
<td>on stack</td>
<td></td>
</tr>
</tbody>
</table>

*Philip Garrou, 3-D ASIP, 2010*
Process Flow: Via Middle & CoW

**FAB Wafer Process**
1. FEOL
2. TSV Formation
3. BEOL
4. C4 Bump Formation
5. Glass Carrier Attach

**Post FAB Wafer Process**
5. Back grinding
6. Passivation
7. TSV Exposure
8. μ-pad

**Assembly & Packaging**
- Tafill
- CoW (chip-on-wafer)
- Glass Detach & Sawing
- Flip Chip Assembly

*Diagram credit: Samsung*
Key Technologies in 3D-TSV

1. Via Process
- High Aspect Ratio Via Filling
- Via Module Integration
  - TSV to FEOL Interaction
  - TSV to BEOL Interaction
- Backside via exposure & passivation
- Yield & Reliability
- Manufacturability

2. Carrier technology
- Attachable/ Detachable
- Small total thickness variation
- Post-fab process compatibility

3. u-Bump joining
- Bump Metallurgy
- Bonding Scheme
- Multi-stacking (Multi-memory)
- Yield, Reliability

4. Flip-chip assembly
- Large die flip chip assembly
- Low-k reliability

5. Thermal

6. Test

7. Design Infra
Via Dimension
: 6um x 55um (50um after thinning)

Via Structure for Logic Applications

- Field Oxide
- TSV (Cu)
- ILD Oxide
- Low-k Dielectric
- M1 TSV Cap
- TSV (Cu)
- O3 TEOS
- Si

Ar milled depth
444um
781um

Wafer thickness
Process Flow: Via Front Side Module

1. Litho
   - PR
   - Si substrate

2. Deep RIE
   - Si substrate

3. Isolation Oxide Deposition
   - Si substrate

4. Barrier/Seed
   - Si substrate

5. Cu Electroplating
   - Si substrate

6. CMP
   - Si substrate
**TSV DRIE**

- Bosch Process: very high selectivity
- Process Challenges:
  - Undercut, Scallop, Via depth uniformity, PR Selectivity, Throughput

**Bosch Process**

- Isotropic etch step
- Polymer deposition step
- Isotropic etch step

- Net anisotropic profile
  - ‘Scallops’
- High net etch rate
- High mask selectivity

**Trade off btw ER and Scallop**

- Longer Step Time
  - Large scallop
  - High etch rate

- Shorter Step Time
  - Smoother sidewall
  - Slower etch rate

*Source: AMAT*
TSV DRIE

Reference

Improved Process; E/R > 10um/min

Top

Middle

Bottom
Most expensive and longest process time

Requirements of Cu Fill

1) Void-free Cu filling
   - Bottom-up fill is not easy
2) Low Cu overburden
3) Low CoO (high throughput)

* Electrolyte chemistry and seed layers are key contributors to the quality of the via filling.
  ➔ Appropriate additive selection will achieve the “bottom-up” fill.

Source: Semitool
Backside Via Exposure

• Total thickness variation (TTV)
  - TTV = Glass + Glue + B/L + Via depth + Si recess etch

• Passivation & planarization
  - Defect-free
  - Cu contamination-free
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Conclusions
Challenges in TSV Integration to Si

- Many concerns in TSV integration into Si
- No Impact due to TSV is a baseline for 3D-IC

- High Aspect Ratio Via Filling
- 3D-TSV Impacts on Devices & BEOL
  - TSV
  - Thin wafer
  - Backside via exposure
  - GWSS process
  - u-bump & stacking process
  - PKG stress
Cu Extrusion

- **Cu extrusion and delamination**
  - CTE difference btw Cu (~17ppm/K) and Si (~3ppm/K)
  - Process temperature of BEOL IMD deposition

![Diagram showing Cu extrusion and delamination](image)

**Step by step Inspection**

- BM/Seed Cu
- EP-Cu
- Cu Anneal
- Cu CMP
- IMD
- TSV module
- BEOL
Power of Cu Extrusion

▪ Examples

• Solid TSV

• Annular TSV

from Tezzaron
Solution for Cu Extrusion

➢ Process Optimization

(a)  
(b)  

TSMC, IEDM 2010
Effects of Via Dimension

- Smaller TSV $\rightarrow$ Less stress & more reliable
- TSV dimension will get smaller because BEOL is getting weaker as scaling

Aspect ratio limit (10:1)
X : delamination

TC 1000 pass

Smaller TSV $\rightarrow$ Less stress & more reliable
TSV dimension will get smaller because BEOL is getting weaker as scaling
TSV Process Impact on Devices

- Vth shift induced by TSV process

- Device performance can be affected by TSV process
- Devices are getting more sensitive; HKMG, Fin FET, Carbon nanotube FET
TSV to Device Interactions

- Device performance change by TSV stress.

![](image1)

Tensile Stress in Silicon

- Stress Measurement using µ-Raman Spectroscopy

![](image2)

R. Geer, IRPS 2011

TSMC, VLSI Symp., 2011
Simulation vs. Experiments

(IMEC, 3D-ASIP 2010)

(TSMC, IITC 2011)
TSV to Device Interactions

TSV proximity impacts on 45nm CMOS devices

Samsung, IITC 2011

<table>
<thead>
<tr>
<th>TSV position</th>
<th>Gate Oxide</th>
<th>Channel</th>
<th>Impact/Impacted distance</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>NMOS</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Vth</td>
</tr>
<tr>
<td>Horizon</td>
<td>Thin</td>
<td>Short</td>
<td>X</td>
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<td>Long</td>
<td>X</td>
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<tr>
<td></td>
<td>Thick</td>
<td>Short</td>
<td>X</td>
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<tr>
<td></td>
<td></td>
<td>Long</td>
<td>+/2um</td>
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<tr>
<td>Diagonal</td>
<td>Thin</td>
<td>Short</td>
<td>X</td>
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<tr>
<td></td>
<td></td>
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<td>X</td>
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<tr>
<td></td>
<td>Thick</td>
<td>Short</td>
<td>X</td>
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<tr>
<td></td>
<td></td>
<td>Long</td>
<td>+/1um</td>
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<tr>
<td>Vertical</td>
<td>Thin</td>
<td>Short</td>
<td>X</td>
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<td>Thick</td>
<td>Short</td>
<td>X</td>
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<td></td>
<td></td>
<td>Long</td>
<td>+/2um</td>
</tr>
</tbody>
</table>

(1) Impact of TSV was observed in less than 2um distance only. The amount of changes caused by TSV were very small, less than 2% in maximum.
(2) Long channel looks more sensitive than short channel.
(3) No impact was found in thin_short_NFET.
(4) No significant impact on off-current.
(5) NMOS looks more sensitive than PMOS.
(6) Regardless of the TSV positions, Idsat is decreased for NFET and increased for PFET by TSV.
Cu Contamination

- **Cu contamination**
  - Device performance degradation by Cu diffusion
  - **Sources**
    - Cu leak through via side wall due to poor liner/BM coverage
    - Cu contamination during backside process
      - Backside passivation
      - Thinned wafer → decrease of gettering layer
Yield of TSV chains with 1000 TSVs
- By eliminating void, > 99% chain yield was achieved
- ~100% yield is required for no test

<table>
<thead>
<tr>
<th>Wf No.</th>
<th>No. Fail</th>
<th>Yield(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
<td>5/1168</td>
<td>99.57</td>
</tr>
</tbody>
</table>
Conclusions

- No impact due to TSV is a baseline for 3D-IC
- There are many obstacles, but 3D-IC is coming soon

Phil Garrou, “The 4 Horsemen of 3D IC, Perspectives from the Leading Edge,”
Oct. 16, 2009