Non-Planar & Non-Si (III-V/Ge) CMOS for High-Performance and Low-Power

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Front End Processes
Outline

• Roadmap

• Technology Strategy
  – Module development
  – Channel architecture

• Results
  – Ge-on-Si high mobility pFET
  – Epi III-V channel on Si
  – High-k gate stack/Junction/Contact modules
  – III-V nMOSFET on Si

• Complimentary Technology
  – III-V for Optical interconnect & Photovoltaic

• Summary
Non-Planar & Non-Si High Mobility CMOS Roadmap

**3D & Non-Si (Ge and III-V) High mobility channel**

- **Si Planar**
- **Si non-planar**

**High Volume Manufacturing**

**Scaling Extension**
- Strain & HK/MG

**INNOVATION**
- Intro. of non-Si high-\(\mu\) channel material

**Metal/ Hi-k dielectric**
- Si/SiGe pMOS Quantum well channel
- Si (100)

**Ge-on-Si Epi defect**
- MOS/HEMT channel
- Ge & III-V CMOS

**InGaAs channel**
- InAlAs / GaAs Metamorphic Buffer
- 4˚ off-cut Si

**III-V on Si Epi defect**
- III-V & Ge CMOS & Photovoltaic

**Photonics to inter connect memory & processor cores**

**Intel IEDM 2007**

**Intel 2011**

**Vdd scaling**
- High frequency

**Power consumption**

- **45nm**
- **32nm**
- **24nm**
- **19nm**
- **15nm**
- **12nm**
- **<10nm**

**2010**
- **2012**
- **2014**
- **2016**
- **2018**
- **2020**
- **>2020**

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FinFET/Tri-Gate scaling Strategy

**Capacitance**
- Fringe to contact/facet
- Low-k spacer

**Pitch Scaling**
- 2nd gen scaling (beyond 14nm)

**Fin/Channel Strain Engr**
- High Mobility Channel
- S/D Stressors (SiGe/Si:C)

**Rext Limitations**
- USJ (Xj~5nm)
- Conformal doping

**Variability**
- Mitigate Random Dopant Fluctuation (RDF)

**Disruptive Gate Stack**
- Higher-k dielectric
- MG WF Tuning

**Contact Resistance**
- High Rco/Rch ratio
- Novel Silicide

**Fin/Gate Fidelity**
- Patterning & Etch
  (prefer 2:1 Gate:Fin)

**Topography**
- Gate/spacer etch
- CMP polish challenge
SiGe-on-Si FinFET Architecture & Results

- Dual channels turn-on cause a kink in CV curve, which reduced in high % of SiGe stack.
- I_dRAIN and Mobility increases as % of H_{SiGe} increases.

Si (40nm)    SiGe (20nm)/Si (20nm)    SiGe (30nm)/Si (10nm)
## Non-Si (High-$$\mu$$) Channel Materials

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InAs</th>
<th>InP</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Electron mobility</strong></td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>40000</td>
<td>5400</td>
<td>77000</td>
</tr>
<tr>
<td>(cm²/Vs)</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td><strong>Electron effective</strong></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mass (/$$m_o$$)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$$m_t$$ : 0.19</td>
<td>m_t : 0.082</td>
<td>0.067</td>
<td>0.023</td>
<td>0.082</td>
<td>0.014</td>
<td></td>
</tr>
<tr>
<td>$$m_i$$ : 0.916</td>
<td>m_i : 1.467</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Hole mobility</strong></td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>500</td>
<td>200</td>
<td>850</td>
</tr>
<tr>
<td>(cm²/Vs)</td>
<td></td>
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</tr>
<tr>
<td><strong>Electron effective</strong></td>
<td></td>
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<tr>
<td>mass (/$$m_o$$)</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$$m_{HH}$$ : 0.49</td>
<td>m_{HH} : 0.28</td>
<td>m_{HH} : 0.45</td>
<td>m_{HH} : 0.57</td>
<td>m_{HH} : 0.45</td>
<td>m_{HH} : 0.44</td>
<td></td>
</tr>
<tr>
<td>$$m_{LH}$$ : 0.16</td>
<td>m_{LH} : 0.044</td>
<td>m_{LH} : 0.082</td>
<td>m_{LH} : 0.35</td>
<td>m_{LH} : 0.12</td>
<td>m_{LH} : 0.016</td>
<td></td>
</tr>
<tr>
<td><strong>Band gap (eV)</strong></td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>0.36</td>
<td>1.34</td>
<td>0.17</td>
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<tr>
<td><strong>Permittivity</strong></td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>14.8</td>
<td>12.6</td>
<td>17</td>
</tr>
</tbody>
</table>

**InGaAs** : High electron mobility (light effective mass) $$\rightarrow$$ nMOSFET

**Ge** : High hole mobility (light effective mass) $$\rightarrow$$ pMOSFET

Band gap, permittivity & density of state ; negative effects.
Hetero-Integration of High Mobility Channel; Key Module & Integration Strategy

Disruptive Gate Stack
- EOT Scaling in the ~5Å Regime (ZIL or Higher-κ materials)
- Low interface trap density (Dit)
- Understanding Mobility Degradation Mechanism @ Scaled EOT

Pitch Scaling Results in Reduced Strain Effects and Increased Contact Resistance which leads to Density-Performance Trade-off.

Low Rco Contacts
- CMOS compatible Contact metals to III-V & Ge S/D
- Interface Engineering for SBH Tuning & high doping
- Advanced TLM test structure for accurate $\rho_{co}$ extraction

Junction & Doping
- Highly doped ultra-Shallow Junction using Mono Layer Doping & Advanced Anneal (Laser/Flash)
- Low Junction Leakage (Ultra-thin channel, silicide, & low Rs)

Epi III-V & Ge Channel
- Selective epitaxy on Si platform
- Low defects density (threading & misfit dislocations)
- Metrology for defect quantification
- CVD epi tool development

New Channel Materials

+ New Silicide Materials

+ New gate stack Materials

High Performance & Low Power Transistor

New Rco Contacts

SI substrate

Pitch

III-V

Ge

High Performance & Low Power Transistor
Hetero-Epitaxy Ge-on-Si & Crystal Defect

Strain relaxed & Defect generation

Defective Epi Ge

Si substrate

Fully strained & defect free SiGe

Critical thickness (nm)

relaxed with defects

metastable

stable

Ge content, x in Si$_{1-x}$Ge$_x$

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39.6nm

79.9nm

50 nm
Ge/ III-V Gate stack & Contact; Low Dit High-k & Low Rco Contacts

Thermal stability of high-k gate on Ge channel

Low contact resistance of Ge pMOSFET

Low Dit high-k on III-V with interface passivation

Mobility of III-V channel Transistor

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Si/SiGe Quantum Well Channel Design

Drain Current ($\mu$A/$\mu$m) vs. Drain Voltage (V) for SiGe MOSFETs with various Si cap thicknesses:
- 0nm Si cap (solid line)
- 3nm Si cap (dashed line)
- 5nm Si cap (dotted line)
- 7nm Si cap (dotted-dashed line)

Log (hole conc.) at different distances from the gate:
- Distance 0nm
- Distance 3nm
- Distance 5nm
- Distance 7nm

Hole $\mu$ ($cm^2/V$-sec) vs. Drain Current ($\mu$A/$\mu$m) for SiGe MOSFETs:
- SiGe PMOSFET (no Si cap)
- SiGe PMOSFET (3nm Si cap)

SiGe pMOSFET (no Si cap):
- $V_G = VT - 0.75V$
- $V_G = VT - 0.25V$
- $V_G = VT - 1.0V$
- $V_G = VT - 0.5V$

SiGe pMOSFET (3nm Si cap):
- $V_G = VT - 0.75V$
- $V_G = VT - 0.25V$

Optimum Si cap confine holes in high-$\mu$ SiGe with good Si Dit.

No Si cap cause high Dit & low $\mu$.

Thick Si cap capture hole in low-$\mu$ Si.

Si cap / SiGe channel QW

Carrier (hole) confined in high-$\mu$ QW

Metal gate

High-k dielectric

Oxide

SiGe channel

Si cap

Si substrate

Optimum Si cap confine holes in high-$\mu$ SiGe with good Si Dit.
Orientation Dependent Transport Mechanism

Substrate orientation & channel direction

Si(100) nFET

V - V_th (V)

Gm Gain Factor

W/L=10/1 |V_d|=50mV

~0 %

Electrons confined in out-of-plane \( \Delta 2 \) valleys are not in-plane direction-dependent.

Si(100) pFET

V - V_th (V)

Gm Gain Factor

W/L=10/1 |V_d|=50mV

8% Anisotropic heavy hole constant energy contour for <100> & <110>. m* of <100> lighter than m* of <110>.

This orientation studies applicable to 3D non-planar transistor architecture

Carrier transport

Si (100) substrate

(110) channel

Substrate orientation & channel direction.
III-V (InGaAs) Channel Design Options

**Architecture #1**

Surface channel (Inversion carrier)

- InGaAs channel
- InAlAs bottom barrier
- InAl-InAlAs graded buffer
- GaAs nucleation and buffer
- 4° (100) offcut Si substrate

(+) CMOS compatible  
(+) EOT & Tinv scaling  
(-) Mobility degradation

**Architecture #2**

Buried channel (Majority carrier, HEMT)

- n++-InGaAs contact
- InP etch stop
- InAlAs top barrier
- Si delta-doping
- InAlAs spacer
- InGaAs channel
- InAlAs bottom barrier
- InAl-InAlAs graded buffer
- GaAs nucleation and buffer
- 4° (100) offcut Si substrate

(+)(+) High channel mobility  
(+)(-) μ less affected by Dit  
(+)(+) High Ion/Ioff (literature)  
(-) Non-self aligned gate  
(-)(-) EOT & Tinv scaling

Electron density vs. Depth from Gate [nm] graph

Electron Density [X10^18/cm^3] vs. Gate [nm] graph
Epi III-V channel Growth on Si Substrate

InGaAs (In=53%~70%) channel nMOSFET

(+): High electron mobility & $\Delta E_{\Gamma-L}$ w/ appropriate $E_g$

(+): Lattice constant matched with InP substrate

(-): challenging 8% lattice mismatch on Si substrate
EOT Scaling: Higher-k & No interface oxide

- Highly scaled CET with no low-k interface for ZrO$_2$ on InGaAs
- Advanced EOT modeling under development to address more accurate quantum mechanical effects in InGaAs

![Graph showing J_g @V_{fb} and CET vs. EOT @V_g = 2V (nm)]

- High-k/SiON/Si
- High-k/Si (ZIL)
- SEMATECH III-V
- EOT (?)
- CET

![SEMATECH III-V image showing ALD TiN, 6.2nm ZrO$_2$, In$_{0.53}$Ga$_{0.47}$As, and CET = 1.06nm]

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High-k on InGaAs with O3 & H2O-based ALD

- H2O-based ALD process improves interface quality (Dit) of ZrO2 and Al2O3
- Low O3 (Lo-O-ZrO2) reduces interface oxidation and CV stretch out

O3-based ZrO2 ALD

H2O-based ZrO2 ALD

H2O-based Al2O3 ALD
Dit Improvement with H2O-based High-k

\[
\frac{I_{cp}}{f} = 2qD_{it}AKT \left\{ \ln \sqrt{t_R t_F} + \ln \left( \frac{|V_{fb} - V_t|}{\Delta V_g} \right) V_{th}n_i \sqrt{\frac{\sigma_p}{\sigma_n}} \right\}
\]

H2O-based high-k have better interface quality than O3-based high-k.
Low Dit H₂O-based high-k ALD process improves FET I-V & Gm as compared to O₃-based high-k ALD for both Al₂O₃ and ZrO₂. These improvements are due to better interface and bulk quality.
SEMATECH actively evaluating [with encouraging results] Si process compatible metals for contacts to III-V in VLSI scheme.
SEMATECH 200mm III-V MOSFET on Si: Using VLSI Si Process Infrastructure

III-Vs can be heterointegrated and processed in same fab as Si
III-V Multi-Junction Solar Cells on Si

III-V CMOS learning re-engaged for III-V photovoltaic

- Hetero III-V epi & bandgap engr.
- Junctions for tandem multi cells
- Low Rc contact for I matching

Multi-junction concentrator III-V PV

Best Research-Cell Efficiencies

High efficiency III-V cell & Low cost on Si platform

Theoretical multi Junction PV

Source: NREL National Renewable Energy Laboratory

*CPV: concentration photovoltaic
High Efficiency/Bandwidth Si Photonics

Si photonics for optical interconnect

Ge-on-Si optical receiver + III-on-Si transmitter (laser)

Planar p-i-n Ge-on-Si photodiode

Laser (λ = 1.3 μm)

CMOS compatible Ge-on-Si optical receiver

Graded SiGe

Si (100)

Ge waveguide photodetector

Transimpedance amplifier

3dB Bandwidth

Response (dB)

Frequency (GHz)

Quantum Efficiency

Bias = 0 V

η_{ext} = 67 % (0.7 A/W)

η_{ext} = 49 % (0.5 A/W)

η_{ext} = \frac{I_{test} \cdot \eta_{calibrated}}{I_{ph}} \cdot \frac{d}{P_o / h \nu}

η_{ext} = \frac{I_{ph}}{q} \cdot \frac{d}{P_o / h \nu}

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Summary

• Non-Si channel (Ge & III-V) transistors overcome fundamental scaling limits with intrinsically high carrier transport

• Outstanding challenges in co-integrating Ge & III-V CMOS on Si platform (Epi, Doping, Gate, Metrology, ESH)

• SEMATECH (Front End Processes; non-Si, test structure, & characterization Teams) work with global partners to address these module issues