Opportunities and Challenges of RRAM

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EOL/ITRI
Classification of Memory Technology

- **Volatile Memory**
  - DRAM
  - SRAM
  - FLASH
  - FRAM
  - Charge-based, Capacitor

- **Non-Volatile Memory**
  - PCM
  - MRAM
  - RRAM (Filamentary)
  - Current-based, Resistor

- **New/Emerging Memories**
  - Charge-based vs. Current-based Operation:
    - Voltage, Current, S/N, Scaling, etc.
  - Filamentary vs. Bulk Conduction/Switching Mechanism:
    - Properties, Size Effect, Scaling, etc.
RRAM Device

1T1R unit cell

Unipolar Switching:
All operations are done at same polarity

Bipolar Switching:
RESET opposite polarity to SET and FORM

Log (Current)

Voltage

Log (Current)

Voltage
RRAM R&D Activities

Published Paper / Year

RRAM

ISI database

Number of papers at the IEDM and VLSI Symposium

Year
Advantages of RRAM

Flash (150°C)
- 0.25V Vth shift 1 hr
- Source: S. Shukuri et al., NVSMW 2008

PCM (180°C)
- ~100% resistance loss <1hr
- Source: ITRI (unpublished)

RRAM (150-200 °C)
- No resistance loss 10 hrs
- Source: H-Y. Lee et al., IEDM 2008

High speed (<300ps)

Fast reading (7.2ns)
Opportunities

• e-Flash replacement

  Issues of e-Flash:
  1. Technology 2~3 generations behind logic
  2. Not compatible with CMOS
  3. Performance not good (speed, endurance)
  4. Not random access

• NOR replacement
• Storage Class Memory (SCM)
• Non-volatile Logic
• NAND replacement?
Memory and/or Storage

**Past**
- AP/CPU: 1 core (>1GHz)
- SRAM
- DRAM (GB)
- Hard Disk (TB)
- Speed, Density and Cost: <ns ns ms

**Present**
- AP/CPU: 2 core (>1GHz)
- SRAM
- DRAM (GB)
- NAND SSD (100GB)
- Hard Disk (TB)
- Speed, Density and Cost: <ns ns us ms

**Future**
- AP/CPU: 4 core (>1GHz)
- SRAM
- Wide I/O DRAM (GB)
- SCM (GB)
- NAND SSD (100GB)
- Hard Disk (TB)
- Speed, Density and Cost: <ns ns 10ns us ms

SCM blurs the boundary of memory/storage
RRAM for NV Logic

- Data Retention
- Speed
- Area

Memristor

NV-SRAM

2011 2012 2013 2014 2015 Year

NV-DFF

NV-Logic

NV-DFF

NV-Counter

Single chip with distributed NVM Circuit

NV-FPGA

• Data Retention
• Speed
• Area
NAND Replacement?

- Now: 20 nm node, 64Gb Floating Gate
- 2022: 8nm node, 512Gb
- All major players will deliver samples of 3D NAND of 1Y generation (~15 nm) next year, but might not go to mass production until 1Z generation, because Floating Gate Flash will still be alive for another generation!
- If 3D NAND lasts for 3 generations, RRAM or any candidates can be introduced at 0Z generation (i.e. ~ 2nm node) around 2026!
Issues to be solved

- Forming
- Electrical Scaling vs. Reliability/Yield
- Switching Device
Time for Forming “Process”

\[ t = \frac{t_{\text{total}}}{M \times N} \]

where \( t_{\text{total}} \): time to form a whole wafer, \( t \): forming time for a single bit, \( M \): Memory size of a chip, \( N \): number of chips per wafer

For an acceptable \( t_{\text{total}} \sim 2 \text{ hrs} \), and assuming a typical 700 gross dies per 12” wafer

\[ t \sim 100 \text{ us/bit for 1Mb chip} \]
\[ 100 \text{ ns/bit for 1Gb chip} \]

Approaches:

✓ Test Engineering:
  a. Increase I/O’s (~10x), b. Apply multi-DUT (10x~100x), c. Increase the applied voltage (\(?x\)).

✓ Device Engineering:
  a. Reduce \( V_{BD} \) (min. \( V_F \)), b. Formingless
Issues:
• Higher current, lower R-ratio
• Poorer reliability
• Smaller process window
Current Scaling

$I = 5\mu A$

$\text{Current} \downarrow \rightarrow \text{Soft error} \uparrow \rightarrow \text{Endurance} \downarrow$
Deterministic vs. Stochastic

Switching Mechanism: Recovery and rupture of the filament (percolation of oxygen vacancy)

High $I_{SET} \rightarrow$ One dominant filament \[\text{Deterministic}\]

Low $I_{SET} \rightarrow$ Several weak filaments \[\text{Stochastic}\]

Process optimization and verification methodology helps to define a dominant filament and thus improves the yield.
(H.Y. Lee et al., IEDM 2010)
Resistance Matching
--- for better reliability

To prevent over-reset problem $V_R$ has to be controlled within a certain range, e.g. 1.5-2.0V

1. After RESET:
$$V_R = \frac{R_H}{R_H + R_{TR}} \times V_{BL} \approx V_{BL} \leq 2V$$

2. Before RESET
$$\frac{R_L}{R_L + R_{TR}} = \frac{V_R}{V_{BL}} \geq \frac{1.5}{2.0} = 0.75 \Rightarrow R_L \geq 3R_{TR}$$

The lower acceptable $V_R$, the higher $R_L$ required.
Choices of the Select Transistor

1T1R unit cell

Transistor for 1T1R RRAM
1. Standard Logic CMOS transistor ~30F2
2. DRAM array transistor for 1T1C 6-8F2 but low current
3. BJT with a better drivability and smaller area offers a better solution (Wang, et al., IEDM 2010)

1BJT1R unit cell
Challenges of Select Device

Sneak current in x-pt structure $\rightarrow$ Selection error

Bi-directional selectors in literatures
1. Self-rectify RRAM, Unity
2. Bi-directional diode (Bi-diode), GIST
3. Complementary resistive switch (CRS), JARA
4. Ovonic threshold switch (OTS), Intel
5. Mixed ionic electronic conduction (MIEC), IBM

Requirement of Selector:
1. On/Off ratio $>> 10^3$
2. Threshold current and voltage match with RRAM operation
3. Process compatibility & Good reliability
Self-rectified 1R Solution

CMOx device, Unity

TaOx/TiOx device, HP

- Simplest structure for high density memory
- LRS nonlinearity and self-compliance are key characteristics.
- No less challenging than finding a well-performed RRAM!!!
Conclusions

- RRAM is a promising memory device for embedded and standalone applications.

- Depending on application and specs., several device and engineering issues have to be solved before mass production is possible. Some feasibility has been proven but data with fine-sized device and large array are critical and required.

- Ultra high density application implies highly scalability with innovative new materials/device structures and is possible only if NAND technology reaches its limit.
Thank you!