Key Technology Challenges for Wide I/O Applications and SEMATECH’s Approaches

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Comparison of wide I/O for mobile and computing (high performance) applications

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[Diagram showing structure comparison]
Reference flow of mobile wide I/O application

Case 1

Logic die (C4 bump face down) → C4 process for Tier 1 → Tier 2 die to tier 1 die attach process → Molding, etc.

Case 2

Carrier → De-bonding → Flip over (C4 bump face down) → Memory + Logic die attach process → Molding, etc.
Comparison of key challenges of cases 1 and 2

<table>
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<th>Case 1</th>
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<td>- Reflow bonding and capillary underfill under 150 µm pitch with thin die (&lt;50 µm) having TSV on laminated substrate</td>
<td>- Debonding of bonded die from carrier after D2D bonding</td>
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<td>- Thermal compression bonding with memory cube</td>
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<td>- Delivery method of memory cube</td>
<td>- Micro bump probing in wafer-level and stacked die (including memory cubes)</td>
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<td>- Wafer-level underfill and bonding (D2D, D2W) without void using wafer-level underfilled die</td>
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<td>- High throughput stacking process</td>
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<td>- Compression molding for TSV die stacked and warpage control for mobile wide I/O application</td>
<td></td>
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<tr>
<td><strong>Metrology</strong></td>
<td><strong>Material</strong></td>
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<tr>
<td>- Inspection after permanent bonding (for bond connectivity and underfill void and so on)</td>
<td>- High thermal conductivity material to control thermal issues</td>
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Reference flow of high performance wide I/O application

Case 1: Logic and memory die attached to Si Interposer (DtI) >>
>> Interposer stack attached to substrate (DtS) >>
>> Backend (heatsink attach/ball attach/singulation)
Reference flow of high performance wide I/O application

Case 2: Interposer attached to substrate (DtS) >>
>> Logic and memory die attached to Si interposer (Dtl) >>
>> Backend (heatsink attach/ball attach/singulation)
Comparison of key challenges of case 1 and 2 for high performance wide I/O

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| - Reflow bonding and capillary underfill under 150 µm pitch with thin die (<50 µm) having TSV on a laminated substrate  
- Thermal compression bonding with memory cube | - Debonding of bonded die from carrier After D2D bonding |
| **Process** | |
| - Delivery method of memory cube  
- Wafer-level underfill and bonding (D2D, D2W) without void using wafer-level underfilled die  
- High throughput stacking process  
- Large and thin interposer handling during bonding | |
| **Test** | |
| - *Micro bump probing in wafer-level and stacked die (including memory cube)* | |
| **Metrology** | |
| - Inspection after permanent bonding (for bond connectivity and underfill void and so on) | |
| **Material** | |
| - High thermal conductivity material to control thermal issues | |
Process: Reflow bonding and capillary underfill under 150 µm pitch with thin die (<50 µm) having TSVs on a laminated substrate (case 1)

- Based on Case 1 reference flow, process is related to bonding of a logic chip on a laminated substrate.
- It is not easy to control warpage with a thin chip and substrate during bonding process.
- It is not easy to handle thin chips with TSVs and microbumps.

Logic die (C4 bump face down) → C4 process for Tier 1 → Tier 2 die to Tier 1 die attach process → Molding, etc.
Process: Thermal compression bonding with memory cubes (case 1)

- During thermal compression bonding, heat should be applied on top of the memory cube. Heat flows can attack bonding metallurgy and other material inside the memory cube.
Process: Delivery method of memory cube

- Memory cube must be transferred from the memory company to OSAT.
- The memory cube may be damaged during delivery.
  - Stacked thin die: It is easy to damage the edge of the top or bottom die
  - If one die is damaged, total memory cube is unusable.
- Memory suppliers may have different approaches to protect the surfaces and edges of memory cubes. This causes OSATs to develop new processes to handle memory cubes. Conventional bare die do not use additional protective layers.
Process: Debonding of bonded die from carrier after D2D bonding (case 2)

- For d2d bonding first, to increase alignment accuracy, a carrier may be needed. After bonding, it needs to be debonded.
- If we do not use a carrier, we need a chucking tool for memory cubes at the bonding machine.
Process: Bonding tool design and bump array cannot cause bump damage of logic chip during thermal compression bonding (Case 2)

Logic die bonding to memory cube
Flip over (C4 bump face down)
Flip over
Carrier
C4 bump of front side
Microbump of logic chip
Face up
Thermal compression tool

Memory + Logic die attach process
Molding, etc.
Process: Wafer-level underfill and bonding (D2D, D2W) without voids using wafer-level underfilled die

- To increase bonding throughput, a wafer-level underfill process is needed.
- To increase reliability using wafer-level underfill, we should develop reliable materials and processes.

Ref.: Jae-Woong Nah* et al., at ECTC 2011

Figure 1. Flip chip bonding process steps with OBAR (over bump applied resin).
Process: High throughput stacking process

- Before stacking (or assembly), most processes are wafer-level processes. So, throughput is high.
- Stacking is a die-level process. Thermal compression bonding especially has very low throughput.
- The stacking throughput should be equal to or higher than the normal 2D flip chip reflow assembly.
Process: Compression molding for stacked TSV die and warpage control for mobile wide I/O applications

- To satisfy the need for thin packages, compression molding will be needed.
- Because of the thin package and molding volume, it is not easy to control warpage.
Process: Large and thin interposer handling during bonding

- Interposer thickness: 50 μm ~400 μm, minimum value is 50 μm
- Interposer size: 25 mm~30 mm (2013), maximum value is 40 mm (2017)
- It is not easy to handle and bond with thin and large interposer
Test: Micro bump probing in wafer-level and stacked die (including memory cubes)

- After bumping, we need to probe micro bumps at the wafer level to verify known good die.
- Before memory cube bonding, we need to verify known good stacked die. For that purpose, a micro bump probe solution for memory cubes is needed.
Metrology: Inspection after permanent bonding (for bond connectivity and underfill void and so on)

- We must find a metrology solution with high resolution and high throughput that is also non-destructive.
Material: High thermal conductivity material to control thermal issues

- If we can use underfill material with high thermal conductivity, we can decrease dummy bumps for thermal conductivity and increase thermal properties of the package.
- Mold compound or passivation material for packages with high thermal conductivity
- Low cost and thin heatsink (if it is needed)
SEMATECH’s approaches

- Standard Activity
- Metrology Evaluation
- Survey of Suppliers’ Readiness
- Process Development
Standard activity

- Standard Activities in Industry
  - 3D-IC Alliance: IMIS™ (Intimate Memory Interface Specification)
  - IEEE - Test: Test Access Architecture for Stacked 3D-Ics(P1838)
  - JEDEC - Test & Design
    - JC-11 Mechanical (Package Outlines) Standardization
    - JC-14 Quality and Reliability of Solid State Products
    - JC-40 Digital Logic
    - JC-40 Digital Logic
    - JC-40 Digital Logic
  - SEMI - Process
  - Si2 – Design
    - Design Exchange for Thermal, Power, Physical, Electrical and Stress Design.
    - Model Formats – Electrical, Thermal, Stress

- 3D Standard Dashboard
  http://wiki.sematech.org/3D-Standards
SEMI® standards: 3D EC leadership

MEMS/NEMS Committee

3DS-IC Committee

North America (R Allen)

Taiwan

Thin Wafer Carrier TF (Rich Allen)

Bonded Wafer Stack TF (Rich Allen)

Inspection and Metrology TF (Victor Vartanian, David Read)

Testing TF

Middle-end Process TF (Jerry Yang)

5175: Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers

5173B: Guide For Describing Materials Properties And Test Methods for a 300 mm 3DS-IC Wafer Stack

5174: Specification for Identification and Marking for Bonded Wafer Stacks

5482: Specification for Glass Wafers for use in Bonded Wafer Stacks (SNARF approved 8/2012)

5269A: Guide for Terminology for Measured Geometrical Parameters of Through-Silicon Vias (TSVs) in 3DS-IC Structures (Ballot Passed)

5270: Guide to Measuring Voids in Bonded Wafer Stacks

5409: Guide for Metrology for Measuring Thickness, TTV, Bow, Warp/Sori, and Flatness of Bonded Wafer Stacks

5410: Guide for Metrology Techniques to be used in Measurement of … Through-Silicon Vias (TSVs) in 3DS-IC Structures

5447: Terminology for Measured Geometrical Parameters of Through-Glass Vias (TGVs) in 3DS-IC Structures (SNARF approved 7/2012)

5473: Guide for Alignment Mark for 3DS-IC Process

5474: Guide for CMP and Micro-bump Processes for Frontside TSV Integration
SEMI® standards: 3D EC leadership

MEMS/NEMS Committee
- 9 Published Standards
Current Activities
- 5 New Standards
- 3 Revisions

MEMS/NEMS Committee

3DS-IC Committee

Wafer Bond TF (Rich Allen)

MEMS Packaging
MEMS Materials Characterization
MEMS Reliability
MEMS Microfluidics
Terminology

Most active TF

MS1-0812: Guide to Specifying Wafer-Wafer Bonding Alignment Targets (Updated version published August 2012)

MS5-1211: Test Method For Wafer Bond Strength Measurements Using Micro-Chevron Test Structures
Support standard activity
- thin wafer handling (D5175) experiment

• Experiment to get data for standards
  – Wafers bonded and thinned to 50 µm/100 µm
  – Wafers debonded and mounted on frames/dicing tape
  – Delivery test
  – Drop tests with packaging

• Simulation for drop test
Packaging options

300 mm wafer
UV-curable dicing tape
SEMI G74 (metal) or G87 (plastic) film frame (diameter = 400 mm)

Multi-Wafer: horizontal and vertical

Single Wafer Stackable: tray and clamshell

Secondary Packaging
Simulation for drop test

Stresses from face drop of wafer on frame

Displacements from face drop of wafer on frame
Metrology evaluation

- Bumped wafers and stacked die used to evaluate metrology solutions
  - Advance 3DIC manufacturability by improving the repeatability, sensitivity, throughput, and CoO of metrology tools.
    1) **C4-bumped and micro-bumped wafers**
       Use inspection and metrology tools to measure micro-bump coplanarity bump height uniformity and detect missing bumps, bridging defects, and contamination.
    2) **Stacked-die assemblies**
       Use inspection tools to detect and characterize underfill voids, striations, defects, delamination, cracks, warpage, and bonding connectivity.

- These test vehicles are on 300 mm wafers.
Metrology evaluation

**Bumped-wafer inspection & metrology**
- Optical: 16 companies

**Die assembly inspection & metrology**
- CSAM: 4 companies
- X-ray: 10 companies
Survey of suppliers’ readiness

• Material (June 2012)
  • EMC (epoxy mold compound)
  • Underfill
  • TIM (thermal interface material)

• OSAT Company (December 2012)

• Interposer Suppliers (December 2012)