Through Silicon Via Testing
Known Good Die (KGD) or Probably Good Die (PGD)

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Advantest
Single Die Fab Yield will drive Cost Equation….

So of course we need to test the die before stacking…. 
Must also consider both Backside Process & Test related Yield...

If Assume Backside Process Yield Loss = 1% (flip chip 1% after 20 years)
If Assume Test Escapes = 1% (let’s discuss today)....

Then...
5 die stack could have 10% final yield loss

The final yield
Yield of single-chip

Number of chips to be stacked
SoC      Memory
**Conventional Test Flow**

- **Wafer Process**
- **Wafer Test**
- **Back Grinder**
- **Dicing**
- **Packaging**
- **Final Test**

**TSV Wafer Test Challenges**

- High Pin Count
- Fine Pitch
- Low Contact Pressure
- Drive-ability
- ESD
- Die Level Completeness
- TSV Check

**Added Test Yield Concerns**
High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness + TSV Check

Limitation: - Current Advanced Probe Cards have Pin Count & Pitch Limits due to MEMS & MLC/Organics

Countermeasures: - Use Dedicated Test Pads, Speed Scan DFT, Correlation based test
- Use Non-contact probing

Issues: - Test Pads take real estate & design time.
- Cannot test I/O characteristics, test pad leakage concerns.
- Non-contact probing requires transmitters and receivers, and power delivery must still be made by physical contact.

Adds Test Yield Concerns
Limitation:  
- Advanced Probe Cards have contact forces ~2g per contact  
- TSV Die may require <1g

Countermeasures:  
- Probe before backside processes (BG, CMP, Etch) or  
- Use Non-contact probing

Issues:  
- Backside processes may induce defects that may go untested.

Adds Test Yield Concerns
Limitation: - Lack of Buffers in device creates drivability problem through fixture to ATE.

Countermeasures: - Active probe cards with buffer amp circuitry.

Issues: - Probe cards require high density circuitry, unproven architecture.

**Adds Test Yield Concerns**
Limitation:
- TSVs create paths to internal nodes of IC not previously exposed.
- Circuit loading may be issue with ESD structures.

Countermeasures:
- Limit ESD in machine model
- Weak, small size ESD flip-flop circuits on IC
- Other: Current trigger and Source Pumping,

Issues:
- Test access point with many switches to TSVs takes lots of space, adds capacitance and requires power.

**Adds Test Yield Concerns**
Drive-ability
High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness + TSV Check

3D clock tree for optimized length and power

Limitation: - If logic is partitioned on different layers, single die may not be fully testable.

Countermeasures: - DFT, Scan Chains
- Comment: IDMs may go this route, but fabless design model may not support repartitioning due to design and software complexities.

Issues: - Not much choice.

Source: Test Strategies for 3D Die-Stacked Integrated Circuits
Lewis & Lee, Georgia Institute of Technology
Highlight:
- High Pin Count
- Fine Pitch
- Low Contact Pressure
- Drive-ability
- ESD
- Die Level Completeness
- TSV Check

Limitation:
- If wafer test before backside processing, TSV cannot be contacted.
- If backside processing before wafer test, no probing or material handling solutions exist for top & bottom side contact.

Countermeasures:
- Use carrier like Film Frame to handle thinned, processed wafers
- Use non-contact (x-ray, infrared, thermography, EM, etc) to inspect TSV structures.

Issues:
- TSVs need to be reliably tested. PPM can have big effect.

Example:
If 1 Die = 1000 TSV
If TSV PPM = 10
Die Yield = 99%

Source: Optimized TSV Filling Process Reduces Cost, Nexx Systems

Add Test Yield Concerns
There are possible solutions to allow continued use of conventional wafer test architecture. They mostly require:

• Silicon Solutions (Test Access Ports & DFT)
• New Probe Card Solutions

These may come at a Test Yield penalty. “Probably Good Die” could become “Maybe Good Die” and unacceptable yield loss at stack.
Conclusion

A Non-Conventional Test Methodology that enables KGD is needed.

- Wafer vs. Singulated Die test
- Zero Force Contacting
- Carrier technologies
- Combined Non-Electrical test
- TSV Top Bottom & Side contacting

→ KGD will be essential to making TSV Stacking cost effective.
Thank You
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