Challenges and solutions for EUV lithography

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Contents

• Lithography roadmap for 2x nm devices and beyond

• Double patterning? EUVL?

• Challenges and solutions for EUVL
  1. Flare Evaluation
  2. Shadowing Effect
  3. EUVL resist process
  4. Feasibility study of EUVL
  5. Future extensions on EUVL
$k_1$ Trends and Lithography technologies

DPT: Double Patterning Technology

- CMOS Metal
- NAND
- 45nm node
- 32nm node
- 22nm node
- 5x nm HP
- 4x nm HP
- 3x nm HP
- 2x nm HP

$1.0NA < k_1 = \text{HP}(N_A/\lambda) < 1.3NA$

- EUVL

Year

Lithography technical road map

hp56nm  hp43nm  hp32nm  hp2xnmxnm  hp1xnmxnm  hp0xnmxnm

ArF IM

- NA > 1~1.35

ArF IM Extend

- Spacer process
- Pattern Split
- Double spacer

EUVL NA0.25 ⇒ NA0.32

Source

Cost

Resist

EUVL Extend

- Spacer Process

Performance & Economics

CD error

Overlay error

Process complexity

Ref T.Higashiki ConFab2010(June) modified
Process flow of double patterning (DP) and EUVL

Double patterning (Spacer process)

Negative type

Mask

Positive type

Resist

Core

Spacer

Space

EUVL

Line
### CDU comparison between EUV and DP

<table>
<thead>
<tr>
<th>Error Assumption</th>
<th>32 nm hp</th>
<th>22 nm hp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Litho CD (3σ)</td>
<td>3.2 nm</td>
<td>2.2 nm</td>
</tr>
<tr>
<td>RIE CD (3σ)</td>
<td>3.2 nm</td>
<td>2.2 nm</td>
</tr>
<tr>
<td>Depo CD (3σ)</td>
<td>2.4 nm</td>
<td>1.7 nm</td>
</tr>
</tbody>
</table>

#### Error components for CD variation [nm]

![Error components for CD variation diagram]

- **Litho**
- **RIE**
- **Depo**

**Target**

**EUV**

- 32 nm hp

**ArF DP**

- 22 nm hp

**TOSHIBA**

Leading Innovation
Various fruits for mass production have been boring on tree of EUV lithography
EUV Focus Areas 2005-2009:

<table>
<thead>
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</thead>
<tbody>
<tr>
<td>1. Resist resolution, sensitivity &amp; LER met simultaneously</td>
<td>1. Reliable high power source &amp; collector module</td>
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<td>1. Long-term source operation with 100 W at IF and 5MJ/day</td>
<td>1. Mask yield &amp; defect inspection/review infrastructure</td>
</tr>
<tr>
<td>4. Source power</td>
<td>4. Reticle protection during storage, handling and use</td>
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<td>• Reticle protection during storage, handling and use</td>
<td>• EUVL manufacturing integration</td>
</tr>
<tr>
<td>• Reticle protection during storage, handling and use</td>
<td>5. Projection and illuminator optics quality &amp; lifetime</td>
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<td>• Projection / illuminator optics and mask lifetime</td>
<td></td>
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EUV symposium 2009 steering committee
Technology contribution of TOSHIBA on EUVL

1. Flare Evaluation
2. EUVL resist process
3. Feasibility study of EUVL
4. Future extensions on EUVL
Flare Evaluation
EUV diffraction by mirror surface roughness

Roughness is defined as deviation from ideal surface.

- **LSFR**: $>1000\,\mu\text{m}$ cycle
- **MSFR**: $1\,\mu\text{m} < \text{MSFR} < 1000\,\mu\text{m}$ cycle
- **HSFR**: $<1\,\mu\text{m}$ cycle

Short range flare
Mid range flare
Long range flare
Amount of flare in EUV systems

Relative intensity of flare

\[ I_{image} = \int f_{image} \]
\[ I_{flare} = \int f_{flare} \]

\[ \frac{I_{flare}}{I_{image} + I_{flare}} = 15\% \text{ in } \alpha \text{ tool} \]
\[ = 8\% \text{ in } \beta \text{ tool} \]

Flare reduction is achieved by improvement of mirror surface.
Flare calculation with PSF, from the scattering position

PSF is provided as radial function as $f(r)$

Flare intensity @ target

\[
\begin{align*}
&= f(R_A) \times \Delta S \\
&+ f(R_B) \times \Delta S \\
&+ f(R_C) \times \Delta S \\
&\vdots \\
&= \iint f(r) dS \\
&\quad S=\text{reflector}
\end{align*}
\]
**Precision – TAT trade off in flare calculation**

**Conventional Flare estimation method**
1. Set mesh on pattern data
2. Calculate pattern density on each mesh
3. Calculate flare magnitude from each mesh

**Flare intensity**

\[
\text{Flare intensity} = f(R_A) \times (\text{pattern density}) \times (\text{mesh size})^2 + f(R_B) \times (\text{pattern density}) \times (\text{mesh size})^2 + f(R_C) \times (\text{pattern density}) \times (\text{mesh size})^2 + \ldots
\]

**Precision and TAT is trade-off in flare estimation.**
To break the trade-off in flare calculation

Mesh size dependence in flare calculations

If we budget 1nm CD error for flare estimation, 0.6% precision is required. We can achieve the precision with 0.25μm mesh, but long TAT is not allowable.

<table>
<thead>
<tr>
<th>Mesh size [μm]</th>
<th>Precision (Error)</th>
<th>TAT (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.25</td>
<td>0.6%</td>
<td>1,296</td>
</tr>
<tr>
<td>0.75</td>
<td>1.5%</td>
<td>16</td>
</tr>
</tbody>
</table>

TAT is estimated with 16 CPUs

T. Uno et al, Photomask Japan 2010

to satisfy both precision and TAT

1. Flexible mesh size with scattering radius
2. Flare compensation on wafer level
Flexible mesh size with scattering radius

In short range
- small mesh size for precision

In long range
- large mesh size to reduce number of mesh

Target precision was achieved in shorter calculation time.
Flare compensation: conventional

Flare calculation

Flare compensation on mask

Design

Mask

Flare map of shot image

Flare Variations among chips

Several number of chip flare correction will be required because of flare variations among chips.

R. Inanami et al, Advanced Lithography SPIE2010
Flare compensation on wafer level

- Flare correction of one chip will be enough for mask level.
- Exposure dose compensation will be carried out at wafer fab, so flexible management can be done with shorter time.

Flare calculation

- Flare compensation on mask
  - High flare
  - Low flare

- No Flare variations among chips
  - High spatial frequency
  - Mask level correction
  - Low spatial frequency
  - Wafer level correction
  - Compensation with exposure dose

- Short range flare
- Long range flare

Design

- Shot
- Chip

Flare map separation

Scattering radius

R. Inanami et al, Advanced Lithography SPIE2010
Exposure Results of Flare compensation

Precise flare compensation ±2.2 nm was obtained through pattern density variation from edge to center of the pattern.

H. Aoyama et al. “Process liability evaluation for EUVL” SPIE vol. 7271-74
EUVL resist process
**CD uniformity on a wafer**

**EUV resist/KrF exposure**

- **Scan-static puddle development**
  - High scan rate: Mean: 144.2nm, 3σ: 5.58nm
  - Low scan rate: Mean: 146.1nm, 3σ: 5.16nm

- **Scan-dynamic dispense development**
  - Conventional: Mean: 146.1nm, 3σ: 5.16nm
  - Optimized: Mean: 144.6nm, 3σ: 3.58nm

**EUV resist/EUV exposure**

- Transfer best process of KrF process
  - Mean: 33.2nm, 3σ: 1.80nm
  - Mean: 34.3nm, 3σ: 1.29nm

S. Ito et al, Advanced Lithography SPIE2010
Scan-static puddle (SP) development

Flow of by-product from exposure area makes localized developer concentration gradient.

- Generate micro loading effect

Scan-dynamic dispense (SD) development

By-product is mixed with new developer instantaneously.
By-product is removed by wafer rotation.

- Micro loading effect of by-product is reduced
Dynamic scan rinse could decrease defect counts by 50% over conventional processes.

S. Ito et al, Advanced Lithography SPIE2010
Feasibility study of EUVL
Test site to evaluate technology maturity

Exposure tool
Mask
Flare compensation
Pattern transfer

Half pitch variation: 43, 38, 35, 32nm

S. kyoh et al, EUV symposium 2009
The cross sectional resist images

Good pattern profiles were obtained for etching hard mask.
The best results of electrical measurements

**Open test site**

- 70% yield was obtained in 35 nm half pitch at 1000 mm length.
- 100% yield was obtained in 35 nm half pitch in 10 mm length.
- Yield was obtained in 32 nm half pitch.

**Conditions**

- The number of evaluated chips are 40 at 43 nm half pitch and 80 at other half pitches.
- The value of resistance within a regulation are recognized as a good chip.
- To evaluate the ability of EUV process, some systematic error of exposure tool was excluded.
Future work for 2X nm hp

Mask

Exposure tool

\[ \sigma_{\text{in}} = 0.4, \sigma_{\text{out}} = 0.8 \]

Resist 26nm 24nm 22nm

Flare & proximity correction

Toshiba
Leading Innovation

S. kyoh et al, EUV symposium 2009
Conclusions

- EUVL has been jumping into the mass-production stage from the stage of basic technology study. However, there remains many technical challenges for further advancement.

- The most critical issues are mask defectivity, source reliability and resist resolutions. Carrying out the EUVL technical development by individual company is impossible. Mutual complements over the world is required to realize next generation’s EUVL.

- Challenges to introduce the successes of mass-production
  - Flare evaluation
    - Flare and shadowing has rather large effects in EUVL comparing with conventional optical lithography. Strict control of those effects will be required.
    - EDA technology shall solve the trade-off between precision and calculation time.
  - EUVL resist process
    - Resolution enhancement and roughness reduction are urgent in resist technology. Infrastructures such as outgas inspection and advanced exposure tool should be prepared as a development platform.
  - Manufacturing integration and future extensions
    - In 3x nm hp, we confirmed successful integration through electrical measurements of test-site. Challenge for a yield in 2x nm hp will be a good exercise of the mass-production.
    - Extendibility of EUVL to 1x nm hp was shown by applying double patterning.
END