Development of 32nm CMOS and Recent Trend for Beyond 32nm

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Content

● **Develop. of 32nm CMOS** - Gate Stack Process
  * Cost effective process
  * High-k material and related process issues (WF)
  * Gate First vs Gate Last (HK first & HK last)
  * Related issues (UT-SiO₂ ,, , )
  * Summary

● **Beyond 32nm Trend** - 2011 Symp. on VLSI Technology
  * VLSI Technology trend
  * Key Issues(FINFET, FD-SOI)
  * Other related topics
    (RTN, 3D-SI, New Ch., TFET, MRAM, BEOL FET,, , )
  * Outlook on future
32nm CMOS

Introduction of
High-k Gate Dielectric
and
Metal Gate Electrode
**EOT Scaling by High-k material**

Scaling limit of SiO$_2$ → Reduction of
- Equivalent Oxide Thickness (EOT)
- Inversion layer Thickness ($T_{inv}$)

$\kappa_{SiO_2} \sim 4$
$\ln(J_G) \propto \frac{1}{T_{ph}}$

$C_{inv} = \frac{\kappa_{SiO_2} \cdot S}{T_{inv}}$

$EOT = \frac{\kappa_{SiO_2}}{\kappa} \frac{T_{phy}}{T_{ph}}$

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**Introduction of High-k/Metal Gate system**

$\nu \gg \nu_{ph}$

$\kappa \sim 20$

$T_{inv} = 0.2\sim 0.5nm$

$C = \kappa \frac{S}{T_{phy}}$

$\nu \propto \exp(-\frac{E}{k_B T})$
Vt mismatch Benefit of High-K Metal Gate

HK-MG improves Vt mismatch
- Historical Poly/SiON Tinv scaling could not overcome LW scaling
- Net Vt mismatch was increasing as scaled technology
- Gate change dramatically improves Vt mismatch

Fig. 1 SRAM Vt mismatch increases as device dimension shrinks. For the first time, the trend is reversed for 32nm node by adopting HK-MG.

H.S. Yang et al., IEDM Tech. Digest, 2008

Courtesy: M. Weybright, IBM

Rama Divakaruni: VLSI 2011 Short Course – Device Technologies for SoC
Gate Stack Options
HK/MG System

PSG
Poly Si Gate

MIPS
Metal Inserted Poly Si Gate

RPG
Replacement Gate

FUSI
Fully Silicided Gate

NECEL
Panasonic
Intel

1st introduction into Market
Potential ability of FUSI

High Potential:
- WF controllability & Cost effectiveness
- No $T_{\text{inv}}$ (MG)

But, tunable WF range is rather narrow
Potential ability of FUSI

- Corrected for slight difference in substrate doping for fair comparison

Reference n-metal and p-metal from B. H. Lee et al., Materials Today, June 2006

- Preliminary results suggest FUSI does not have $V_{FB}$ roll-off
- Could be due to absence of high T steps after FUSI
Optimum Work Function

- $I_{dsat} @ target I_{off} = 100\text{nA/um (HP)}$
- $I_{off} = 1\text{nA/um (LOP)}$
- $I_{off} = 10\text{pA/um (LSTP)}$

**Optimum WF**

- **NMOS**
- **NiSi**
- **Ni$_{31}$Si$_{12}$**

**WF [eV]**

- 4.0 4.2 4.4 4.6 4.8 5.0 5.2

**$I_{off}$**

- ~4.05
- ~5.15
FUSI CMOS Flow

e.g. 100 nm

Simultaneous silicidation

NiSi (NMOS)

Ni$_3$Si (PMOS)

PN Boundary Issue

NiSi

Ni$_3$Si

Ni  Ni

Poly-Si

Si  HK

NMOS  PMOS
High-k Gate
Dielectric Materials
Ionic Bond vs Covalent Bond

**Transition Metal**;
Low ionization energies having a positive oxidation states

![Diagram of Ionic Bond and Covalent Bond]

**HfO₂**

**SiO₂**

Compared to SiO₂ (strong covalent bond), HfO₂ has lot of Oxygen vacancy and this leads to essential influence on FET characteristics.

How to control of Oxygen vacancy is essential issue for HK/MG system
FLP Phenomenon

Oxygen in HfO$_2$ moves into Poly Si resulting in Oxygen vacancy ($V_o^{2+}$) in the HfO$_2$

⇒ Electric Dipole formation at the interface ⇒ $V_{fb}$ shift

K. Shiraishi et al., VLSI Tech. Symp. 2007
How to obtain the intrinsic $V_{fb}$ value

$$V_{fb} (meas.) = V_{fb} (int.) + \Delta V_{fb} (Q_{fix})$$

$$\Delta V_{fb} = d Q_{fix} / S \varepsilon + (1/2) d^2 Q_{fix} / S \varepsilon$$

EOT = 0 $\Rightarrow$ d = 0

**Slant Etch preparation**

**Metal Gate**

**Important regime!**
Effective Work Function (eWF)

A charge “+q” at distance of d in the HK modulates WF by 
\(-q(d/\varepsilon) \Rightarrow “eWF”\)

\[ \Delta V = -\frac{1}{\varepsilon} \int \rho(x) dx = -\frac{q \cdot d}{\varepsilon} \]

Band edge WF MG is necessary, however, Interfacial reaction (FLP, \(V_{th}\) roll-off) at MG/HK and HK/IL causes dipole and fixed charge

**Retrograded Work Function**

(Effective WF: eWF)

**Challengeable against EOT scaling**

**V_{th}** lowering and Process Integration are Antithetical concepts!!
WF control by capping
Dipole formation

- Various kinds of capping materials
  LaO, MgO, DyO, AlO, TiO, ...

- Capping process
  Ex.
  Dielectric: ALD 2.5nm
  HfSiO+DPN+PNA
  Thermal budget: 1030°C

- Allocation of capping
  Above HK
  Below HK
Deterioration of WF due to (interfacial) reaction (Dipole Formation; FLP, $V_{fb}$ Roll-off)

Gate(HK) First Process

Deterioration of WF due to (interfacial) reaction (Dipole Formation; FLP, $V_{fb}$ Roll-off)

FLP (Fermi Level Pinning)

$V_{fb}$ roll-off

eWF (effective Work Function)

Complexity

Low Vth

SMDD
1 metal
2 dielectrics

DMSD
2 metals
1 dielectrics

DMDD
2 metals
2 dielectrics

S: Single, M: Metal, D: Dual, D: Dielectric

Antithetical btw Integration and $V_t$ lowering!
Integration Issue

W effect

Concern of Oxygen penetration

STI

NMOS

L

STI

PMOS

Poly Si

TiN

STI

Active

Active

SiO₂

Active

M.Niwa

110622 SMT Symp.
Comprehensive understanding of oxygen behavior
Scaling of MG/HK including IL

Possible explanation;

- For thick IL: \( \text{O}^{2-} \) HK \( \Rightarrow \) MG
  To compensate generation of \( V_o^{2+} \), \( \text{O}^{2-} \) in IL \( \Rightarrow \) HK

- When IL becomes thinner:
  Less \( \text{O}^{2-} \) IL \( \Rightarrow \) HK

- For ultra-thin IL: \( \text{O}^{2-} \) in HK \( \Rightarrow \) IL

S.C. Song et al., IEDM 2007
**V_{fb} modulation by capping material**

Oxygen density determines direction and strength of produced dipole.

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**Fig. 1.** Experimentally observed $V_{fb}$ shift caused by high-k/SiO$_2$ interface dipole formation for Al$_2$O$_3$/SiO$_2$, HfO$_2$/SiO$_2$, Y$_2$O$_3$/SiO$_2$, and La$_2$O$_3$/SiO$_2$.

**Fig. 3.** Areal density of oxygen atoms ($\sigma$) in various oxides, normalized by that in SiO$_2$ ($\sigma_{SiO2}$).

Oxygen density is different from each material.

K. Kita et al., IEDM 2008
Start Commercial Shipment of 32nm-CMOS with HK/MG in Sept. 2010

Panasonic to Start Commercial Shipment of 32-nm Generation System LSIs Based on World's First† Gate-First, High-k/Metal Technology

Osaka, Japan - Panasonic Corporation has successfully developed a new mass-production technology for leading-edge 32-nm generation system LSIs, and is ready to ship system LSIs (model number: MN2WS0150) based on this technology from October 2010 for use in Blu-ray Disc™ players. This advanced technology enables system LSIs with higher performance and lower power consumption to be used for consumer electronics including digital TVs, Blu-ray Disc™ recorders and players.

As the market for new consumer electronics, such as Blu-ray 3D Disc™ players, is rapidly growing, there was an urgent need for a mass-production technology that can support low-power, high-performance microscopic transistors on 32-nm or later generation system LSIs.

The world's first† technology Panasonic has developed for fabricating high-k/metal gate transistors in a gate-first process can significantly improve CMOS transistors' performance by up to 40% compared to its current models. The MN2WS0150 system LSI, featuring 32-nm generation transistors and Panasonic's proprietary Uniphier®3 integrated platform for digital consumer electronics, is designed for Blu-ray Disc™ players which are compatible with Blu-ray 3D™ discs. The newly-developed technology enables reducing LSI's power consumption by approximately 40% and the mounting footprint by 30% compared to the current models by employing high-density integration of the microscopic transistors and power consumption control according to the LSI's operations.

Panasonic's advanced 32-nm generation system LSIs have been realized based on the following technologies:
1. New CMOS process technologies4 for multi-Vth based on new gate
Transistor Features

- 35 nm min. gate length
- 160 nm contacted gate pitch
- 1.0 nm EOT Hi-K
- Dual workfunction metal gate electrodes
- 3rd generation of strained silicon
45nm High-k + Metal Gate Strain-Enhanced FETs
(Intel)

Since PMOS 1st, NMOS process is free from P-metal stress

SiGe channel & Gate Last →Δµ(hole): +50%

C. Auth et al., VLSI Tech. Symp. 2008
Intel 32nm Logic FET
Gate Last (HK Last)

NMOS

PMOS

Dec. 2009 Press release: Processor 「Westmere」
～ March. 2010 PC with this CPU[Xeon] was on the Market
Issue on HK last process (CMP Process)

Planarization, STI bump height, (Non-)Silicidation area

Conventional process

CMP1 (PSG planarization)

CMP2 (PS denudation)
Issue on HK last process (Multi-Oxide)

HK first: Multi-oxide is used as IL
HK last: Precise control of remaining oxide thickness after Gox removal is key issue

HK first:
- Core
- I/O
- HK/MG/PS
- PS removal

HK last:
- PS depo.
- PS/Gox removal
- Chem.Ox./HK/MG

Optimization of remaining oxide thickness after Gox removal is crucial.
# Summary

## Contributing factor of $V_{th}$

### Gate Last

<table>
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<tr>
<th>HK last</th>
<th>HK 1st</th>
<th>Gate 1st</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>?</td>
<td>Yes</td>
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### $V_{fb}$ Roll-off

<table>
<thead>
<tr>
<th>HK last</th>
<th>HK 1st</th>
<th>Gate 1st</th>
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</thead>
<tbody>
<tr>
<td>None</td>
<td>None</td>
<td>Yes</td>
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### FL Pinning

<table>
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<tr>
<th>HK last</th>
<th>HK 1st</th>
<th>Gate 1st</th>
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</thead>
<tbody>
<tr>
<td>None</td>
<td>Yes</td>
<td>None</td>
</tr>
</tbody>
</table>

### Remark

- **WF:** Ideal
- **Scaling:**
- **Metal Etch back:**
- **Cost:**

### Counter measures:

- **WF:** Problematic
- **Cost:**

### Summary

- Band Edge WF but complex: Suitable for HP
- Low cost but less band edge: Suitable for LOP/LSTP
Ultra-thin Oxide thickness

$\text{SiO}_2$ is still a key dielectric

As Interfacial Layer for HK/MG system, BD mechanism of Bi-layer system (HK/IL), Host gate dielectric of 28nm CMOS for LOP, , ,
Physical Structure  

XTEM image  

Si Sub.  

polySi  

SiO₂  

1.39 nm  

Strained layer  

Fresh  

Si Sub.  

Broken-down  

Reliability  

Gate  

SiO₂  

Vg  

M.Niwa  

110622 SMT Symp.
Breakdown phenomena of HK/MG stack

BD mechanism depends on Dielectric and Gate electrode
(⇒ needs new criteria)


* SILC is controlled by the trap generation in the primarily near its interface with HK.
* MIN (w/o IL) do not exhibit an appreciable SILC up to the BD moment.

G. Bersuker et al., IEDM 2008

Base oxide layer for high-k
Zero Interface

\[ \Rightarrow \quad EOT : \downarrow \quad \text{Mobility} : \downarrow ? \]
Specific PVD formation; “Hf-metal sputter + RPO; Scavenging technique”

Hf-metal_sputter: pure Hf-metal can be deposited uniformly and in high density.

RPO: the Hf-metal can be oxidized uniformly with oxygen radicals and referentially against Si interface at specific low temperatures.

Beyond 32nm CMOS

2011 Sym. On VLSI Technology @ Kyoto

+ α
Keywords from 2011 Symp. on VLSI Technology

New Channel on Si
3D Approach
Nanowire
Adv. Memory
Spintronics
TFET
RTN
FINFET
SOI
FinFET Challenges

- Parasitic resistance increasing [1,2]
- Larger gate to source/drain capacitance [3]

### Bulk FET vs. FIN FET

<table>
<thead>
<tr>
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<th>Bulk FET</th>
<th>FIN FET</th>
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<tbody>
<tr>
<td>$V_{th} = V_{FB} + \psi_s (inv) + \frac{q N_{sub} W_{dep}}{C_{ox}}$</td>
<td>$V_{thDG} = \phi_m + V_{thDG} \left( n^+ - Si \right)$</td>
<td></td>
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<tr>
<td>where $V_{FB} = (\phi_m - \chi_{Si} - E_g / 2)$</td>
<td></td>
<td></td>
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<tr>
<td>$\sigma(V_{th}) = \frac{q}{C_{ox}} \sqrt{\frac{N_{sub} W_{dep}}{3LW}}$</td>
<td>$N_{sub} \Rightarrow \text{None}$</td>
<td></td>
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<tr>
<td>$\propto \frac{T_{ox} \sqrt{N_{sub} W_{dep}}}{\sqrt{LW}} \propto \frac{T_{ox} N_{sub}^{0.25}}{\sqrt{LW}}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\sigma(V_{th}) \propto \sigma(\phi_m)$</td>
<td>$\sigma(V_{th}) \propto \sigma(\phi_m)$</td>
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<tr>
<td>$\propto \frac{1}{\sqrt{LW}}$</td>
<td>$\propto \frac{1}{\sqrt{LW}}$</td>
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</table>

**FINFET;**

Due to its strong carrier controllability,

1) Punch-through can be easily suppressed  
   ⇒ SCE can be suppressed further  ⇒ Better scalability

2) Lower $N_{sub}$ ⇒ Smaller variability ($V_{th}$)

Due to the same operating principle as Ultra-thin FD-SOI!

**FIN-width** ($W_{\text{fin}}$) should be shorter than $L_g$ ($W_{\text{fin}} < L_g/2$)
Press release by Intel; May, 2011

New Transistor Grows in the Third Dimension
Transistor Innovations Enable Technology Cadence

- **2003**: Invented SiGe Strained Silicon
- **2005**: 2nd Gen. SiGe Strained Silicon
- **2007**: 2nd Gen. Gate-Last High-k Metal Gate
- **2009**: First to Implement Tri-Gate
- **2011**: 22 nm

Strained Silicon

High k Metal gate

Tri-Gate

Transistor Operation

- **Channel Current (normalized)**
- **Gate Voltage (V)**
- **Reduced Threshold Voltage**

The steeper sub-threshold slope can also be used to target a lower threshold voltage, allowing transistors to operate at lower voltage to reduce power and/or improve switching speed.
Tri-gate nanowire MOSFETs
M. Saito, et. al., Toshiba, Tokyo Inst. of Tech.

1. Universal line appears in Pelgrom plot of both $V_{th}$ and $I_d$ variations of nanowire transistors.
2. $A_{vt}$ in NW Tr. is lower than planar Tr. due to gate grain alignment.
3. $I_d$ variations can be reduced by improving side-surface roughness.

![Diagram](image)
A 0.021 \mu m^2 trigate SRAM cell with aggressively scaled gate and contact pitch

IBM Research, IBM T.J. Watson Research Center, Yorktown Heights, NY

**LATE NEWS**

Fig 12: $I_d - V_g$ curves for CMOS devices taken from a 0.025 \mu m^2 cell, 60 nm CGP

Fig 13: Demonstration of a 0.025 \mu m^2 bitcell with a CGP of 60 nm and CFP of 50 nm.

Fig 5: SEM images showing highlighted cells after completion of spacer formation. The highlighted region in each image indicates the extent of the cell. Numbers correspond to (1) pull up (2) pull down and (3) pass gate FETs for a half cell. The scale bar corresponds to 200 nm.

Fig 6: TEM images of a 0.021 \mu m^2 cell showing the (a) gate cross section and (b) fin cross section. (1) BOX (2) fin (3) NiPt siltide (4) poly-Si (5) SiN spacer (6) TaN gate metal and Hf-based gate dielectric. The physical gate length is 15 nm and fin width is 7 nm. The scale bar corresponds to 50 nm.
Multi $V_t$ demonstration by FDSOI-HK/MG CMOS with Back gate bias

For advanced SRAM, FD-SOI is very promising candidate to suppress the variability. However, Bulk Si is still necessary for the peripheral circuits which need large current, i.e., ESD protection or Power MOSFET. Need for the hybridization of FD-SOI & Bulk Si is becoming popular since 2009.
20nm ETSOI CMOS and SRAM
K. Cheng, et. al., IBM, STMicroelectronics, GLOBALFOUNDRIES, Renesas, Toshiba

1. First demonstration of 20nm ETSOI CMOS with 22 nm gate length, and sub-100 nm contacted gate pitch
2. 25% improvement in speed over 28nm bulk low power technology.
3. High density 6-Transistor SRAM cells down to 0.08 µm² cell size.
4. Competitive drive currents: (NFET/PFET) of 1150/1050 µA/µm at Ioff = 100 nA/µm for high performance (HP); and 920/880 µA/µm at Ioff = 1 nA/µm for low power (LP), respectively, at VDD = 1 V.
5. Auxiliary ETSOI devices including epitaxy resistors with high precision and gated diodes with near ideal characteristics are fabricated on ETSOI to enable early ETSOI SoC design.
50nm FDSOI 3D-integrated CMOS
P. Batude, et. al., CEA-LETI

1. 3D sequential integration enable 3D interconnections at the FET scale (CMOS can be vertical)
2. Thanks to its high alignment performance ($\sigma<10\text{nm}$), it allows the full use of the 3rd dimension potential.
3. First demonstration of 3D sequential integration with $L_G=50\text{nm}$
4. Molecular bonding is used to obtain perfect top active layer (crystalline quality and thickness)
5. Low temperature FET ($<650\degree\text{C}$) appears viable for scaled FETs
1. An aggressively scaled high-k last metal gate (HKMG) stack was successfully implemented for 20nm high performance and low power applications.

2. Key achievements are
   (a) aggressive Tinv scaling down to 1.1nm
   (b) suppression of Vfb roll-off for good control of PMOS Vt
   (c) replacement metal process with suitable Vt and good Vt uniformity
   (d) metal gate stress engineering for transistor performance improvement
Tunnel FETs for extremely low power application
U. Avci, et. al., Intel

1. TFET is a leading device option for low power in the beyond CMOS era
2. Steep I-V turn-on characteristic if realized enables low supply operation
3. Analysis of process variation impact on the TFET shows it is no worse than CMOS
4. Circuit assessment of TFET logic is compared to CMOS Logic. TFET Logic shows 8x higher performance than CMOS for extremely low-power applications.

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<th>Switching Energy (fJ)</th>
<th>Leakage Power (nW)</th>
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<tr>
<td>Combined</td>
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<td>Combined</td>
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<td>0.46</td>
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</table>
ETB III-V-On-Insulator MOSFET
S.-H. Kim, et. al., The University of Tokyo

1. First operation of Extremely-thin body (ETB) MOSFETs with metal S/D in III-V MOSFETs
2. High mobility with ETB less than 10 nm by using In$_x$Ga$_{1-x}$As with high Indium contents (0.7) and inserting In$_{0.3}$Ga$_{0.7}$As (large band gap) buffer layer
Process Variation Source

- Ox thickness
- Fix charge
- Defects and traps
- Work function variation within device

Variation source

- Random Dopant fluctuation
- High-K Metal gate
- Line edge roughness
- Implant and anneal
- Pattern roughness (CMP)
- Polishing uniformity (CUP)
- Strain
- N/P patterning

Figure 3A: An example of a design process layout with the effects of several factors on the success of a post-critical process variation in metal.
Assessment of the situation in technology is a key issue!

*Important message on recent 28nm CMOS for LOP application!*

With appropriate $T_{\text{inv}}$ scaling by SiON/PS, high speed & low power consumption can be achieved at the same time!
A 28nm Poly/SiON CMOS Technology for Low-Power SoC Applications


Advanced Technology Division of Logic, United Microelectronics Corporation Ltd. (UMC)
Tainan Science-Based Industrial Park, Tainan 74147, Taiwan
Spintronics: Magnetic Tunneling Junction is implemented onto CMOS

Fig. 1 TEM images of 28nm MTJ cells well patterned at 5F pitch with no side wall damage (a) and 2F pitch with by-products on side wall (b)

Fig. 11 Scalability of MTJs. With current spec. MTJ (FL 21Å and AR 3), 28nm is the scaling limit theoretically. For 1X nm level MRAM requiring Ic of 19µA, a novel FL material with substantially low Jc needs to be developed.

At VLSI Circ. Symp., Tohoku Univ. + NEC have developed the World’s First Content Addressable Memory that Stores Data without using Power!
VLSI Technology Trend

2006, STRJ (Semiconductor Technology Roadmap committee of Japan)

Evolution of Si System By introducing new Materials, Structure and Design

3D Integration

Between CMOS Elements

New technologies

Beyond CMOS Elements

Explorative Research

Design Enablement

Heterogeneous Integ.
Technology Evolution

New evolution beyond 32nm
EUV Litho. ↔ Immersion Litho. + DP
Tr: Planar MOS ↔ Multi Gate, SOI, 3D

Year

Cost / Function
Performance

32-28nm
22nm
< 20nm
> 45nm

ArF Enhancer

ArF immersion

Low k
k=2.7

Cu
L=35nm

Low k
k=3.0

SiGe
L=35nm

strain

metal gate

high -κ

SoGe

300nm

Silicide

USJ

> 45nm

SMO
Double Patterning

EUV Double Patterning

Immersion Litho.

Tr: Planar MOS

Multi Gate, SOI, 3D

Fab-less Tool

3D TSV

3D

EUV Litho.

< 20nm
Ge/II-Ⅴ+Si-MOSFET; High-performance & Multi-function by Heterogeneous integ.

High speed by Hybridization

Ultra-low power by TFET

Multi-function by Heterogeneous integration

S. Takagi, VLSI 2010
Thank you !