3D TSV Program Overview

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3D TSV outlook

• Near future (2011 - 2013)
  – Interposer products
  – Wide IO DRAM (mobile)

  – Heterogenous integration (beyond memory on logic)
  – Higher (>> 5 stacking levels)
  – Smaller (<< 5 micron width, >> 10 aspect ratio)

• Far future (2017 - 2025)
  – Beyond CMOS (photonics, sensors, etc)
SEMATECH survey on gaps in the via-mid ecosystem

- 12 companies surveyed Aug-Sep 2010: IDMs, foundries, fabless, OSATs
- High density via-mid applications including interposers, heterogeneous stacking, logic on logic, memory on memory; 2011-2014 timeframe
- Addresses all aspects of via-mid: wafer processing, assembly, reliability, inspection/metrology, design, test
- Highest priorities for heterogeneous stacking (e.g., wide IO DRAM) shown below

Gaps in Standards and Specifications

- EDA Exchange Formats
  - Partitioning and floorplanning; Logic verification; Power/Signal integrity analysis; Thermal analysis flow; Stress analysis flow; Physical verification; Timing analysis
- Reliability
  - Reliability test methods
- Test
  - DFT test access architecture
- Inspection/metrology
  - TSV voids, defect mapping, microbump inspection and coplanarity
- Chip Interface
  - Stackable memory pin assignment; Stackable memory physical pinout
- TSV
  - Keep out area, fill materials, dimensions
- Thin wafer handling
  - Universal thin wafer carrier

Technology Development and Cost Reduction

- Reliability
  - Criteria; Test methods; ESD
- Temporary bond/debond cost reduction
  - Materials and release mechanisms cost reduction; Equipment cost reduction
- TSV
  - Keep out distance/area
- Microbumping and bonding
  - Pad metallurgy and layer thickness; Bump metallurgy
- Inspection/metrology
  - Microbump inspection and coplanarity; TSV voids; BWP voids
- Test
  - Probing microbumps cost reduction
Program organization

Core: GF, HP, IBM, Intel, Samsung, TSMC, UMC, CNSE

Program Member: Hynix

Unit Process
- TSV Module
- Thin
- Bond
- Metrology

Module Development
- Baseline/Yield
- Device Interaction
- Reliability
- Modeling/Simulation
- Test Vehicles

Enablement Center
- Standards
- Metrology/Inspection
- Microbumping/bonding
- Industry gaps

Associate Members
- Atotech, Lasertec, NEXX, TEL, COSAR
- ADI, Altera, ASE, LSI, NIST, ON, Qualcomm

Reference Flows
- Standards, Specs

Core Program

Unit processes
- Equipment development
- Integration
- Test Structures
- Early reliability
Scope of technical TSV program

Materials:
- Liner, barrier, seed
- Plating chemistry
- Bond materials
  - Temporary, tack
  - Permanent

Equipment Development

Unit Process Development
- TSV Module
- Bond Module
- Thin and handle
- Backside processing

Metrology
- Infrared
- Acoustic
- X-ray techniques
- Standard techniques

Integration
- Passive TSV daisy chains
- TSV DtW daisy chains
- Device interactions
  - 65nm and 30 nm planar/non-planar
  - Keep out area
- Thermo-mechanical modeling/simulation
- Electrical modeling/simulation
- Early reliability

Thermo-Mechanical Modeling/Simulation

Micro-Chevron

Electrical modeling/simulation

Early reliability

Thermo-Mechanical modeling/simulation

Micro-Chevron
3D equipment capability

- **Bonding**
  - Wafer Align/Bond (manual)
  - Wafer Align/Bond (automated)
  - Die align/bond (automated)

- **3D Metrology**
  - Scanning Acoustic Microscope
  - Thickness Monitor (capacitance)
  - IR Microscope
  - All Surface Inspection
  - TSV depth metrology
  - Access to AFM, SEM, TEM, HRP, etc via ISMI & CNSE

- TSV RIE
- Multicell Cu Plater
- Wafer background
- Wet hood for cleans and chemical thinning
- Spin/bake (materials characterization)
- Tabletop debonder (thermal slideoff)
- Reliability (EM, TDDB, SV, TC at CNSE)

Access to state of the art FEOL/BEOL tooling for standard CMOS processing and metrology at CNSE
Die to wafer bonding

Yielding TSV chains and DtW/TSV chains demonstrated
Mean Kelvin resistance of equals unbonded, damascene reference
Established capability for evaluating tools, materials, unit processes, modules and reliability
Overview of key 3D contributions

• Established 3D Enablement Center
  – Develop industry standard reference flows
    • Appropriate test structures and data generation from the core program
  – Identify gaps in 3D HVM & drive infrastructure readiness for HVM
  – Drive consensus in the industry to minimize cost and risk

• Established baseline R&D capability to explore 3D materials, process and equipment issues
  – Complete 300mm 3D tooling, metrology and reliability capability
  – Yielding TSV/DtW chains (test bed for bonding, materials and metrology)

• Supplier collaborations to develop tool/material infrastructure

• Materials screening to down select options

• University collaborations for special capabilities and skills
  – Bond materials, thermomechanical modeling, metrology, reliability

• Addressed issues requested by member companies, identified gaps,
  – Fostered consensus: surveys, workshops, advisory groups
  – Access to SEMATECH tools through demo requests from members
3D Enablement Center - background

• SIA survey by technology strategy committee identified 3D as a focus area

• Goals:
  – Jump start the 3D industry
  – Demonstrate SIA leadership
  – Be industry member driven
  – Leverage SEMATECH/SRC capabilities

• Activities:
  – Industry wide standards orchestration (standards dashboard)
  – Reference flow(s) development
  – Development of inspection/metrology specifications
  – Microbump/bond metallurgy specifications
  – Near term university research (SRC)
  – Industry gaps

SEMATECH, SIA and SRC Team to Establish New Collaborative Program for Enabling 3D ICs

Industry pulls together to develop industry standards to guide 3D integration and accelerate technology adoption

Albany, NY and WASHINGTON (December 8, 2010) – SEMATECH, the Semiconductor Industry Association (SIA), and Semiconductor Research Corporation (SRC) announced today they have established a new 3D Enablement program to drive cohesive industry standardization efforts and technical specifications for heterogeneous 3D integration. Through the guidance of SEMATECH working in partnership with SRC, the program aims to establish the infrastructure necessary for the industry to leverage 3D packaging technology for innovative new applications.
Overall 3D Enablement Center vision

Industry consensus building on standards and specifications in Phase 1

Phases 2 - 4 represent opportunities to address gaps in the EDA and test vehicle space
2011 workshops
(Identifying gaps and consensus building)

- Design for Reliability Workshop – Stress Management for 3D ICs Using Through Silicon Vias
  - March 17, 2011, Santa Clara, CA
- SEMI MS5 - Test Method for Wafer Bond Strength Measurements Using Micro-Chevron Test Structures
  - July 11, 2011, SEMICON West
  - Standards Technical Education Program (STEP)
- SEMATECH Workshop on Bonding
  - July 11, 2011 SEMICON West
- Joint SEMI/SEMATECH workshop – 3D standards
  - July 12, 2011, SEMICON West.
  - Committee/task forces meetings (morning); Open meeting (afternoon)
- SEMATECH Workshop on 3D Interconnect Metrology
  - July 13, 2011, SEMICON West
- Product-Level Reliability Workshop – Stress Management for 3D ICs Using Through Silicon Vias
  - July 14, 2011, SEMICON West
- Future - Stress Management for 3D ICs Using Through Silicon Vias
  - Fall 2011, TBD
Summary

• Capable, well established program
  – Complete 300mm equipment capability
  – Excellent representation across industry through members and suppliers

• Participation in the 3D program provides
  – Reference flows
  – Models: Thermomechanical, Electrical, reliability, cost …
  – Data for model validation
  – Industry trends and standardization
Accelerating the next technology revolution

Research  Development  Manufacturing

SEMATECH