CMOS Scaling Beyond FinFETs: Nanowires and TFETs

Chris Hobbs, Wei-Yip Loh, Kerem Akarvardar, Paul Kirsch, and Raj Jammy
June 22, 2010
Outline

- Advanced CMOS Scaling Overview
- Nanowires
- TFETs
- Summary
Device scaling options

\[ I_{d,\text{sat}} \]

\[ V_g \]
Device scaling options

\[ I_{d,\text{sat}} \quad \text{vs} \quad V_g \]
Device scaling options

- Very high mobility/high injection velocity
  - SiGe, Ge, InGaAs
  - Graphene [$\mu_e \sim 15000 \text{ cm}^2/\text{V-s at RT}$]
Device scaling options

- Very high mobility/high injection velocity
  - SiGe, Ge, InGaAs
  - Graphene [$\mu_e \sim 15000 \text{ cm}^2/\text{V-s at RT}$]
- Better electrostatic control
  - Multiple gates + more channel area
  - FinFETs, nanowire FET
Why are Multi-Gates beneficial?

- Thin silicon channel with gate on both sides helps maintain channel control.
- Source and drain are much closer...
  Gate loses control of channel region
  • Thin silicon channel with gate on both sides helps maintain channel control.
Performance and power tradeoff

- Same transistor with specifications tuned for performance or power @ cost.
Performance and power tradeoff

All Face Transistor Scaling Issues (need new materials/architectures/novel processes)

Typical Ion-Ioff for CMOSFETs

- HP CMOS (High performance)
  - Highest $I_{on}$, Lowest CV/I
  - High leakage
  - Medium $V_{dd}$

- LOP CMOS (Low operation power)
  - Lowest $V_{dd}$
  - Medium $I_{on}$, medium CV/I
  - Medium leakage

- LSTP CMOS (Low standby power)
  - Lowest leakage
  - Low $I_{on}$, high CV/I
  - High $V_{dd}$

- Same transistor with specifications tuned for performance or power @ cost.
MOSFET scaling trends

Planar

High-K

45nm
(Production)
Intel IEDM 2007

32nm
(Production)
Intel IEDM 2009

New materials


Si-Ge Device

22nm?
IBM, IEDM 2009

16nm?
6nm Length
B. Doris IEDM 2002

III-V Device


12nm+
SEMATECH, IEDM 2007,9

SEMATECH, IEDM 2010

Non planar

• **Past:** Performance improved by scaling device dimensions.

• **Now:** Performance improved by Novel Materials and Architectures.

• **Planar CMOS and Beyond:** A continuous spectrum of devices.
Non-planar devices

Motivation:
- Gate wrap-around helps control short channel effects in scaled devices
- High mobility channels enables higher drive currents

Scaling Pathways

Bulk vs SOI

w and w/o 3rd gate?

Homogeneous

OR

Heterogeneous

OR

High $\mu$

11 June 2011
Critical FinFET/Trigate/Nanowire Modules

- Most nanowire module issues are similar to FinFET module issues with added degree of integration complexity.
Silicon Nanowires

$W_{mask} = 50 \text{ nm}$

suspended wires

source

drain

450 nm

$W_{mask} = 50 \text{ nm}$

450 nm

$|V_D| = 50 \text{ mV}$

$|V_D| = 1 \text{ V}$

Gate length = 40 nm
NW width = 50 nm
NW height = 20 nm

14 June 2011
Gate wraparound improves rolloff

- Nanowire device has smaller rolloff compared to FinFET.
  - Wrapping gate around channel improves short channel control.

- Long channel SS is similar for Omega-Gate and FinFET.
  - $V_{dd}$ scaling limited by SS.
  - Different device structure needed to reduce $V_{dd}$. $\rightarrow$ TFET!

- Gate-All-Around (GAA) Device:
  - Total current in nanowire limited by crosssectional area.
  - Multiple GAA nanowires to meet ITRS targets.
  - In contrast, total current in FinFET can be increased with taller fins.
Stacked Si nanowire formation using SiGe

- Stacking nanowires helps increase total drive current to meet ITRS targets.
High mobility SiGe FinFETs/nanowires

- SiGe PFETs have higher mobility than Si fins.
- Potential for performance > strained Si in non-planar devices
Outline

- Advanced CMOS Scaling Overview
- Nanowires
- TFETs
- Summary
Device scaling options

- **Very high mobility/high injection velocity**
  - SiGe, Ge, InGaAs
  - Graphene [$\mu_e \sim 15000 \text{ cm}^2/\text{V-s at RT}$]

- **Better electrostatic control**
  - Multiple gates + more channel area
  - FinFETs, nanowire FET

- **Improve on-off ratio**
  - Tunnel FET
    - Very steep $\Delta S \ll 60 \text{ mV/dec}$
    - Low bias voltages ($\ll 1\text{V}$)
  - Nano Electro Mechanical switch (NEMS)
    - Hybrid: $I_{on}$ by CMOS + $I_{off}$ by NEMS
    - Zero Leakage Power
Device scaling options

- **Very high mobility/high injection velocity**
  - SiGe, Ge, InGaAs
  - Graphene [$\mu_e \sim 15000 \text{ cm}^2/\text{V-s at RT}$]

- **Better electrostatic control**
  - Multiple gates + more channel area
  - FinFETs, nanowire FET

- **Improve on-off ratio**
  - Tunnel FET
    - Very steep $\Delta SS \ll 60 \text{ mV/dec}$
    - Low bias voltages ($\ll 1\text{V}$)
  - Nano Electro Mechanical switch (NEMS)
    - Hybrid: $I_{on}$ by CMOS + $I_{off}$ by NEMS
    - Zero Leakage Power
V_	ext{CC} scaling for “green” electronics

- Passive power has shown continuous increase due to V_{DD} scaling limit.
- V_{CC} scaling limited by V_T and subthreshold slope (which is kT/q limited)
  \[ \rightarrow \text{need “green” devices not governed by } kT/q \sim 60\text{mV/dec limit.} \]
Working mechanism of TFET

**MOSFET:**
- For Narrow On/Off Voltage Range:
  - Low Ion → Low I_{off}
  - High Ion → High I_{off}
- Electrons go over thermionic energy barrier
- Boltzmann distribution of carriers causes leakage.

**TFET:**
- Carriers go through the energy barrier.

Band-to-Band Tunneling, SS < 60mV/dec
Several types of TFETs with Si PIN, Metal Schottky PIN, and Si-pocket PIN have been demonstrated.

Ultra-low subthreshold of < 50 mV/dec has been achieved over a 10^3 order of magnitude for drive current.

Very Low SS, need more Ion.
**N_D activation for high I_on Si TFET**

- Highest $I_{on}$ (~109 $\mu$A/\(\mu\)m) at $V_{cc} = 1.0V$ for Si TFET using optimized flash anneal for $N_d$ activation.

- Good Ion, poor SS.

---

**References**

6. 40th ESSDERC 2010, p162

---

**Table:**

<table>
<thead>
<tr>
<th>References</th>
<th>Channel Material</th>
<th>SS (mV/dec) @ RT</th>
<th>$I_{on}$ ($\mu$A/(\mu)m)</th>
<th>$V_{ds}$ (V)</th>
<th>Ion/Ioff$^\dagger$</th>
</tr>
</thead>
<tbody>
<tr>
<td>S. Mookerjea [1]</td>
<td>InGaAs</td>
<td>150–290</td>
<td>20</td>
<td>0.75</td>
<td>$&gt;10^3$</td>
</tr>
<tr>
<td>T. Krishnamohan [2]</td>
<td>Si</td>
<td>460</td>
<td>$10^4$</td>
<td>1.00</td>
<td>$&gt;10^2$</td>
</tr>
<tr>
<td>F. Mayer [3]</td>
<td>Ge</td>
<td>&gt;400</td>
<td>4</td>
<td>0.80</td>
<td>$&gt;10^2$</td>
</tr>
<tr>
<td>F. Mayer [3]</td>
<td>Si</td>
<td>42–200</td>
<td>0.04</td>
<td>0.80</td>
<td>$10^5$</td>
</tr>
<tr>
<td>K. K. Bhuwalka [4]</td>
<td>Si</td>
<td>285</td>
<td>0.1</td>
<td>1.50</td>
<td>$10^4$</td>
</tr>
<tr>
<td>W. Y. Choi [5]</td>
<td>Si</td>
<td>52.8</td>
<td>12$^*$</td>
<td>1.00</td>
<td>$10^4$</td>
</tr>
<tr>
<td><strong>This work [6]</strong></td>
<td>Si</td>
<td>120–250</td>
<td><strong>84</strong></td>
<td>0.70</td>
<td>$&gt;10^5$</td>
</tr>
</tbody>
</table>

$^\dagger$Ion is taken at overdrive of $V_g-V_{BT} = 2.0V$ except for $^\ast$. Ion/Ioff taken at onset of BT-BT, $V_{BT}$
E\textsubscript{g} engineering : H-TFET

- Effective E\textsubscript{g} can be engineered by using heterostructure (e.g. Ge on Si)
- Ge % from 25 ~ 50% \(\rightarrow\) Bandgap engineering to enhance tunneling
- Abrupt doping gradient by in-situ B-doped SiGe and post annealing

\[\text{Heterostructure TFET}\]

\[\text{Ec offset and bandgap narrowing for high tunneling}\]

\[\text{Much lighter Hole mass}\]

SEMATECH-UCB DARPA Joint Project
III-V tunnel FETs

- Tunneling is a strong function of bandgap.
- III-V has smaller bandgap and heterostructures (e.g. InAs/Al$_x$Ga$_{1-x}$Sb) have staggered or even zero bandgap → direct tunneling.
- Preliminary InGaAs TFETs results indicates further optimization is needed to improve the poor SS, high $I_{off}$, high Dit and poor $R_{co}$. 

Novel design: pocket structure TFET

- Large field, good capacitive coupling btw gate & pocket
- Abrupt turn-on due to overlap of valence/conduction bands
- Tunable turn-on voltage

[C. Hu et al, VLSI-TSA, April, 2008]
Dopant-segregated Si-pocket TFET

- Achieved sub-60 mV/dec (46 mV/dec) with 30% dies showing sub-60 mV/dec Si TFET with high-K/MG.
S-MLD pocket InGaAs pocket TFETs

- N+/p- pocket structure achieved on InGaAs TFET.

- Enhanced drive current obtained due to enhanced vertical field at gated pocket n-p+ junction.

- Improved gate coupling and Dit observed.
Simulation of TFETs

IV TFETs (Simulation)

IIIIV TFETs (Simulation)

[1] C. Hu et al. (invited), VLSI-TSA 2008
Current TFET performance

- Experiments show higher sub-threshold slope than simulations.
- No physical demonstration of TFET with both high \( I_{on} > 100 \, \mu A/\mu m \) and SS < 60 mV/dec has been demonstrated so far.
Summary

• Power Constrained CMOS Scaling requires new materials and device structures to enable continued scaling.

• Nanowires:
  – Better short channel control than FinFETs with added degree of integration complexity

• TFETs:
  – Band to band tunneling transport mechanism allows for sub-60mV subthreshold slope
    → Vcc reduction → lower power consumption
  – TFETs simulations show promise for Vcc reduction and additional process improvements are needed to improve device performance.