3D TSV Metrology Challenges

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Our thoughts on 3D Life (in general)
3D TSV outlook

- **Near future (2011 - 2013)**
  - Interposer products
  - Wide IO DRAM (mobile)
    - Performance, power, footprint & cost

  - Heterogenous integration (beyond memory on logic)
  - Higher (>5 stacking levels)
  - Smaller (<5 micron width, >10 aspect ratio)

- **Far future (2017 - 2025)**
  - Beyond CMOS ( photonics, sensors, etc)
Mobile wide IO DRAM

3D Metrology Needs:

TSV Module
- TSV dimension, depth and profile
- Liner/barrier/seed thickness
- Defects: fill voids, delamination, protrusions

Bond Module
- Overlay
- Bond voids
- Interface defectivity
- Wafer warpage and stress

Thinning Module
- In line wafer thickness control
- Backside TSV height (reveal control)

Microbump
- Microbump height co-planarity
- Microbump metallurgy
Our capabilities …
3D metrology capability

- **In house Tools**
  - Scanning Acoustic Microscopy (bond voids)
  - Infrared Microscopy (alignment, defectivity)
  - TSV depth measurement
  - Atomic Force Microscopy (TSV heights)
  - Micro-Raman (stress measurement in silicon)
  - TEM (interfaces, stress in silicon)
  - Capacitance (wafer thickness, warp/bow)
  - All surface inspection (wafer edge, front/backside)
  - Particles, SEMs, etc

- **Demo capability**
  - Xray tomography (via voids)
Lasertec TSV300-IR confocal microscope

Image courtesy Lasertec, Inc.

Measurement optics

Static repeatability

<table>
<thead>
<tr>
<th>Wafer A</th>
<th>Die position on the wafer</th>
<th>Average Depth [μm]</th>
<th>3 sigma [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 μm Via</td>
<td>Center</td>
<td>10.25</td>
<td>0.02</td>
</tr>
<tr>
<td></td>
<td>Right</td>
<td>10.03</td>
<td>0.01</td>
</tr>
<tr>
<td></td>
<td>Left</td>
<td>10.09</td>
<td>0.02</td>
</tr>
<tr>
<td>1 μm</td>
<td>Center</td>
<td>10.79</td>
<td>0.02</td>
</tr>
<tr>
<td>Isolated</td>
<td>Right</td>
<td>10.77</td>
<td>0.05</td>
</tr>
<tr>
<td></td>
<td>Left</td>
<td>10.82</td>
<td>0.04</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Wafer B</th>
<th>Die position on the wafer</th>
<th>Average Depth [μm]</th>
<th>3 sigma [μm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 μm</td>
<td>Center</td>
<td>50.47</td>
<td>0.04</td>
</tr>
<tr>
<td>Isolated</td>
<td>Right</td>
<td>48.36</td>
<td>0.06</td>
</tr>
<tr>
<td></td>
<td>Left</td>
<td>48.52</td>
<td>0.04</td>
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<tr>
<td>5 μm</td>
<td>Center</td>
<td>50.54</td>
<td>0.05</td>
</tr>
<tr>
<td>Dense</td>
<td>Right</td>
<td>48.59</td>
<td>0.03</td>
</tr>
<tr>
<td></td>
<td>Left</td>
<td>48.34</td>
<td>0.06</td>
</tr>
</tbody>
</table>

Results by 10 time measurement

Achieved a good repeatability for high aspect ratio via of 1 μm and 5 μm.

Images courtesy Lasertec, Inc.
What we’re doing about it…
### SEMATECH metrology evaluations

#### Table 10  TSV Etch Depth and Profile Metrology Assessment

<table>
<thead>
<tr>
<th>Technique</th>
<th>5 micron TSV</th>
<th>1 micron TSV</th>
<th>Destructive</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Depth</td>
<td>Profile</td>
<td>Depth</td>
</tr>
<tr>
<td>Cross-section SEM</td>
<td>Red</td>
<td>Green</td>
<td>Red</td>
</tr>
<tr>
<td>FIB-SEM</td>
<td>Red</td>
<td>Green</td>
<td>Red</td>
</tr>
<tr>
<td>Optical Microscope</td>
<td>Yellow</td>
<td>Red</td>
<td>Yellow</td>
</tr>
<tr>
<td>Backside IR interferometry</td>
<td>Red</td>
<td>Green</td>
<td>Red</td>
</tr>
<tr>
<td>White Light Interferometry</td>
<td>Red</td>
<td>Green</td>
<td>Red</td>
</tr>
<tr>
<td>IR Confocal</td>
<td>Yellow</td>
<td>Red</td>
<td>Yellow</td>
</tr>
<tr>
<td>IR Interferometry</td>
<td>Red</td>
<td>Green</td>
<td>Red</td>
</tr>
<tr>
<td>Model Based IR Reflectometry</td>
<td>Red</td>
<td>Green</td>
<td>Red</td>
</tr>
<tr>
<td>TSOM</td>
<td>Red</td>
<td>Green</td>
<td>Yellow</td>
</tr>
</tbody>
</table>

#### Table 1  SAM Supplier Landscape

<table>
<thead>
<tr>
<th>Scanning Acoustic Microscope</th>
<th>Overlay</th>
<th>Voids</th>
<th>Defect</th>
<th>Inspect</th>
<th>Review</th>
</tr>
</thead>
<tbody>
<tr>
<td>Manual SAM</td>
<td>Red</td>
<td>Red</td>
<td>Red</td>
<td>Red</td>
<td>Red</td>
</tr>
<tr>
<td>Auto SAM (dry in/dry out)</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
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</tbody>
</table>

#### Table 2  IR Supplier Landscape

<table>
<thead>
<tr>
<th>IR Microscope</th>
<th>Overlay</th>
<th>Voids</th>
<th>Defect</th>
<th>Inspect</th>
<th>Review</th>
</tr>
</thead>
<tbody>
<tr>
<td>IR defect review tool</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
</tr>
<tr>
<td>All surface inspection</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
</tr>
<tr>
<td>IR microscope overlay tool</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
<td>Green</td>
</tr>
</tbody>
</table>

- Red = No
- Green = Yes
- Yellow = Maybe
Consensus building

- SEMATECH Workshop on 3D Interconnect Metrology
  - July 15, 2009 (SEMICON – West; San Francisco, CA)
  - July 14, 2010 (SEMICON – West; San Francisco, CA)
  - July 13, 2011 (SEMICON – West; San Francisco, CA)

- Industry collaborations
  - ITRS
  - SEMI®
  - NIST
SEMI® 3D standards activities

New 3DS-IC Committee and Task Forces Formed December 2010

SEMI®

MEMS/NEMS Committee

3DS-IC Committee

Silicon Committee

23 Committees total

... Thin Wafer Carrier TF (Urmi Ray)

5175: Guide for Multi-Wafer Transport and Storage Containers for Thin Wafers

Bonded Wafer Stack TF (Rich Allen)

5173: Specification for Parameters for Bonded Wafer Stacks

5174: Specification for Identification and Marking for Bonded Wafer Stacks

Inspection and Metrology TF (Chris Moore)

Initial focus on the physical parameters of TSVs

Carrier wafers Edge trimming (Proposed)

Initial focus on the dimensions and sizes of carrier wafers as well as edge trimming of device wafers
3D Enablement Center

- Program announced December 2010 by SEMATECH, SIA, and SRC
  - Designed to meet diverse needs of SIA members: high performance, mobile, analog, mixed signal, MEMS, fabless, fablite, IDMs
  - Address gaps identified in SEMATECH industry-wide survey

**SEMATECH, SIA and SRC Team to Establish New Collaborative Program for Enabling 3D ICs**

*Industry pulls together to develop industry standards to guide 3D integration and accelerate technology adoption*

*Albany, NY and WASHINGTON (December 8, 2010) – SEMATECH, the Semiconductor Industry Association (SIA), and Semiconductor Research Corporation (SRC) announced today they have established a new 3D Enablement program to drive cohesive industry standardization efforts and technical specifications for heterogeneous 3D integration. Through the guidance of SEMATECH working in partnership with SRC, the program aims to establish the infrastructure necessary for the industry to leverage 3D packaging technology for innovative new applications.*

- Mission:
  - Enable industry-wide ecosystem readiness for cost effective TSV-based 3D stacked IC solutions

- Members include:
  - **Enablement Center**: ASE, Altera, ADI, LSI, NIST, ON Semi, and Qualcomm
  - **3D Program**: Hynix
  - **SEMATECH Core**: CNSE, GlobalFoundries, Hewlett Packard, IBM, Intel, Samsung, TSMC, and UMC
3D Enablement Center

- Primary focus is on Wide IO DRAM for mobile applications
  - Provide clarity to help identify gaps in standards, specifications, technologies
  - Also explore high performance computing, others

- Activities:
  - Reference Flow development
  - SEMI® Standards and Standards Orchestration
  - Development of Inspection/Metrology specifications
  - Microbump/bond metallurgy specifications
  - Near term university research (SRC)
  - Industry gaps

- Future programs under consideration:
  - Pathfinding
  - EDA tools
  - Test vehicles
Program organization

**Core:** GlobalFoundries, HP, IBM, Intel, Samsung, TSMC, UMC, CNSE

**Program Member:** Hynix

**Unit Process**
- TSV Module
- Thin
- Bond
- Metrology

**Module Development**
- Baseline/Yield
- Device Interaction
- Reliability
- Modeling/Simulation
- Test Vehicles

**Enablement Center**
- Standards
- Metrology/Inspection
- Microbumping/bonding
- Industry gaps

**Associate Members**
Atotech, Lasertec, NEXX, TEL, COSAR

**Members**
ADI, Altera, ASE, LSI, NIST, ON, Qualcomm

**Reference Flows**
- Standards, Specs

**Unit processes**
- Equipment development
- Integration
- Test Structures
- Early reliability
Overall 3D Enablement Center vision

Goals:

- Jump start the 3D industry
- SIA-SEMATECH-SRC partnership
- Identify industry gaps
- Be industry member driven
- Leverage SEMATECH/SRC capabilities and resources of industry/government
Accelerating the next technology revolution

Research

Development

Manufacturing

SEMATECH