Metrology for FinFET, High Mobility III-V FET & Emerging ReRAM Devices

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(for FEP division)
Outline

• MOSFET Scaling Overview
• Non-Planar Devices
• High Mobility Channels (III-V)
• Resistive RAM (ReRAM)
• Summary
Generic MOSFET Scaling Trends/Innovations: Novel Materials and Architectures

New Mat’l/Structure

- **High-K**
  - **MG**
  - **45nm**
  - **2007**

- **Planar**
  - **32nm**
  - **2009**

- **Tri-Gate**
  - **22nm**
  - **2011**

- **16nm (?)**
  - **2013+**

**Non-planar**

- **T-FET**

- **III-V Device**
  - **Intel, IEDM 2007, 9**

- **Si-Ge Device**

- **Nano-wire** (LETI IEDM’08)

- **3D-NWFET**

**Past:** Performance improved by scaling device dimensions.

**Now:** Performance improved by Novel Materials and Architectures.
Junctions

**Conventional Planar Device**

- Halo & Extensions used to control SCE
- Extension doping < deep S/D doping

**FinFET**

- Double gate & fin width reduces SCE
- Would like:
  - Uniform current at top and bottom of fin → uniform S/D doping
  - Low resistance → Full dopant activation
TEM with EDX from baseline

- **Challenge:** How to quantify dopant concentration
Sims result on baseline

- B dopant seems to be low, work with CNSE on calibration
- Good match with SVTC and NIST data on low doping now, the scaling on high dope is still off

Sims outline:
Fill implanted FINFET space with Si

Sims data for FINFET Baseline

- As concentration 25keV
- B concentration 4keV shifted X axis by 31.85

Lower dopant concentration come from side wall and average over the space filled with poly Si
Scanning capacitance microscopy

- NIST* develop carbon nano-tube tip enable scanning of AFM and SCM

Sample preparation and SCM outline


*TD#100065104A-ENG : ISMI and NIST SEMATECH confidential
HRXRD SiGe/Si Fin Strain Direction Dependence

- The as-grown SiGe epitaxy layer is strained.
- Etching SiGe/Si fins results in strain relaxation along the fin width but not along fin length.
- HRXRD provides useful information to understand the evolution of strain in devices.

24 June 2011

SEMATECH confidential
Nanobeam Diffraction to Map Fin Strain

- Nanobeam diffraction provides useful qualitative understanding of how strain varies within a device.
- FinFET device with SiGe/Si stacked fin has strain present in SiGe layer.

STEM deflection system scan along line

Collect series of filtered diffraction patterns along line.

Software analysis of successive diffraction patterns positions calculates change in structure due to strain.

28nm Si

13nm SiGe

Collaboration with FEI/Metrology Division
11 nm Module: Junction requirement

- **Hetero-buffer**
  - $\mu_n > 10000 \text{ cm}^2/\text{Vs}$ @ $n_s \sim 5e12 \text{ cm}^{-2}$; defect density $\sim < 1e6 \text{ cm}^{-2}$; thickness $< 0.2 \mu\text{m}$

- **Gate Stack**
  - EOT $< 1 \text{ nm}$, $D_{it} < 1e12$, $V_{th}$

- **Junctions**
  - Shallow extensions for SCE control and low $R$ - $X_j < 10 \text{nm}$, $R_{sh} < 200 \text{ ohm/sq}$

- **Contacts**
  - CMOS Metals, $\rho_c < 1\Omega.\text{um}^2$

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Slide from Richard
# III-V junction characterization scheme

- **High Resolution XRD** [1,2]
  - ![High Resolution XRD](image)
  - **2112.54A In % 51**
  - **252.33A In %53**
  - **InP**

- **Raman spectroscopy** [3,4]
  - ![Raman spectroscopy](image)

- **Hall measurement**
  - ![Hall measurement](image)

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<th>Material or process parameter</th>
<th>HRXRD</th>
<th>Raman</th>
<th>Sims</th>
<th>Hall measurement</th>
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<td>Dopant activation</td>
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<td>Crystal quality</td>
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<td>Mobility</td>
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<td>Dopant profile</td>
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- Capable provides quantitative data
- Not capable
- Capable but limited to qualitative data

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![Figure from http://en.wikipedia.org/wiki/Semiconductor_carrier_mobility](image)

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## Defect density monitoring

<table>
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<tr>
<th>Material or process parameter</th>
<th>X-ray diffraction imaging (XDI)</th>
<th>High resolution XRD (HRXRD)</th>
<th>Raman</th>
<th>TEM</th>
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<tbody>
<tr>
<td>Defect density</td>
<td>![Green Circle]</td>
<td>![Orange Circle]</td>
<td>![Green Circle]</td>
<td>![Orange Circle]</td>
</tr>
</tbody>
</table>

**Table Key:**
- Red circle: Not capable
- Orange circle: Capable but limited to qualitative data
- Green circle: Capable provides quantitative data

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**Image from SiGe:**
- Show crack

**X-ray Red-model:**
- Black-data

**Clear fringes in HRXRD:**
- Indicates good crystal quality
- FWFM signal can be calibrated by defect density from TEM

**Forbidden signal (To-GaAs):**
- Because of poor crystal quality of GaAs grown on Si

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Ge on Si
- Top view
- Cross section

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21 March 2011
Asymmetric RRAM bipolar behavior

Reset with “good” RRAM dielectric against Anode

Tunnel barrier quickly and easily forms during reset against “good” dielectric

Reset with “poor” RRAM dielectric against Anode

Too many easy leakage paths during reset………
> can not form barrier

ALD HfO2 + OEL
Controlled Asymmetric Stoichiometry

PVD ~20nm HfO + various O exposure + Pt cap

- ~4nm PVD HfO2 dep
- 240s O*
- 35s O*
- Atmosphere exposure
- As-dep

O signal for all

Backside SIMS

TiN\20nm HfOx\TiN

Tunnel barrier quickly and easily forms if reset against “good” dielectric
Summary

• CMOS scaling requires new materials and device structures to enable continued scaling.

• New challenges for metrology include:
  – Fin characterization
  – Gatestack uniformity
  – Junction characterization
  – Stress measurements
  – Defect measurements
  – Material characterization